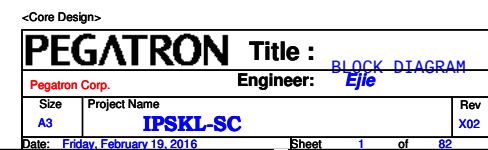
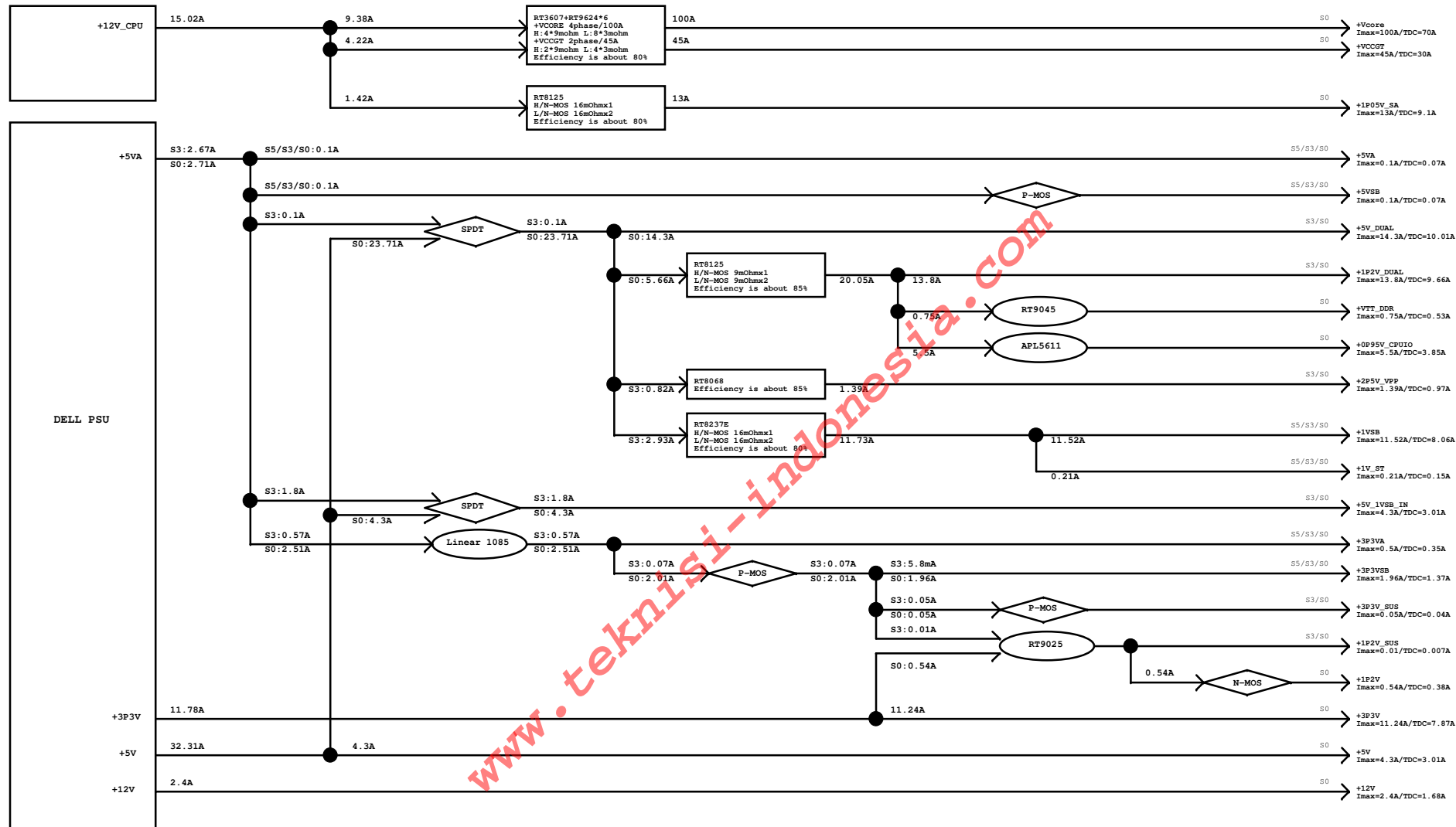


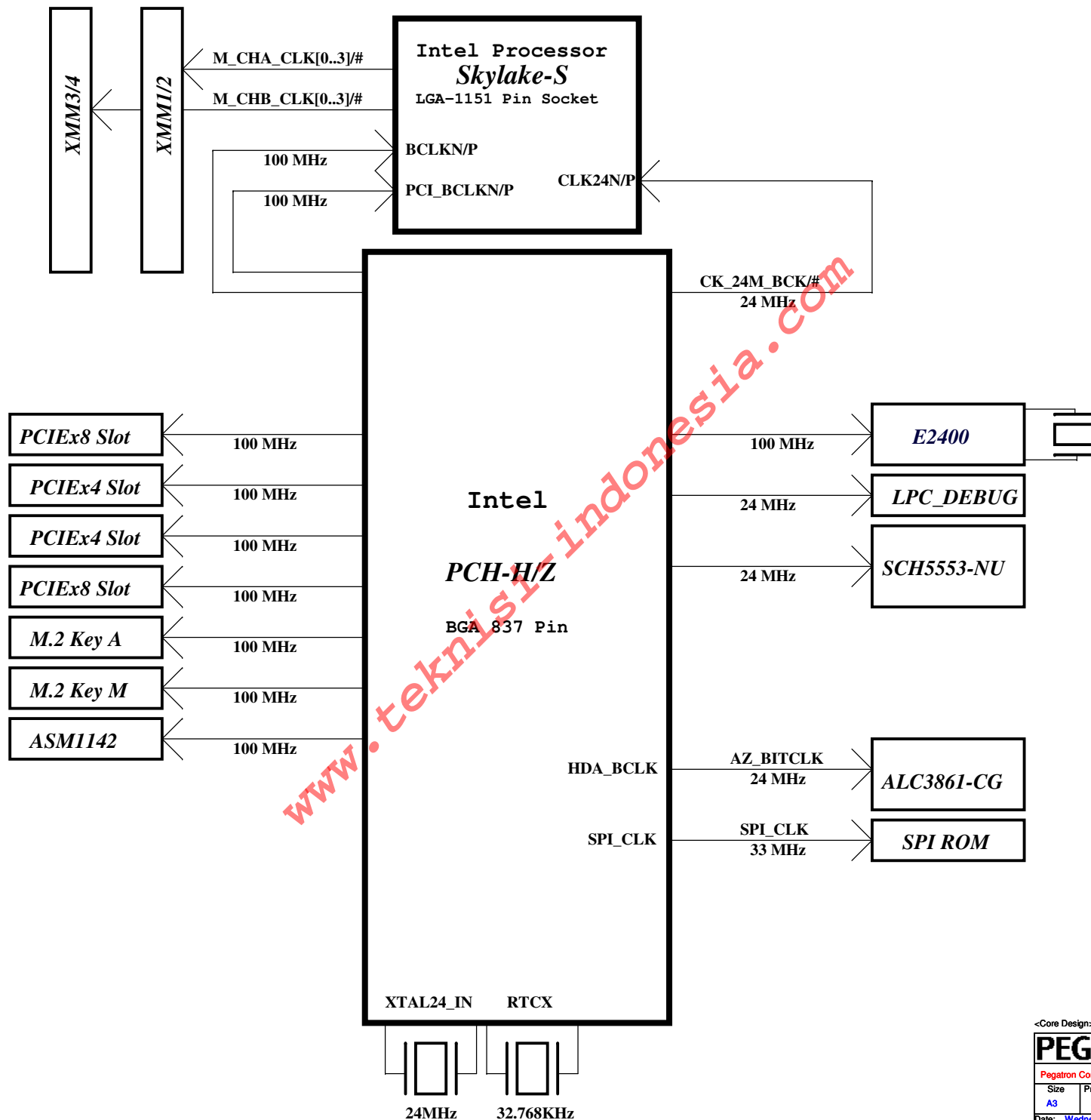
Revision: X02

79	REAR USB 2.0 X4 CONN
80	USB CHARGE
81	REAR AUDIO CONN
82	LED DRIVER

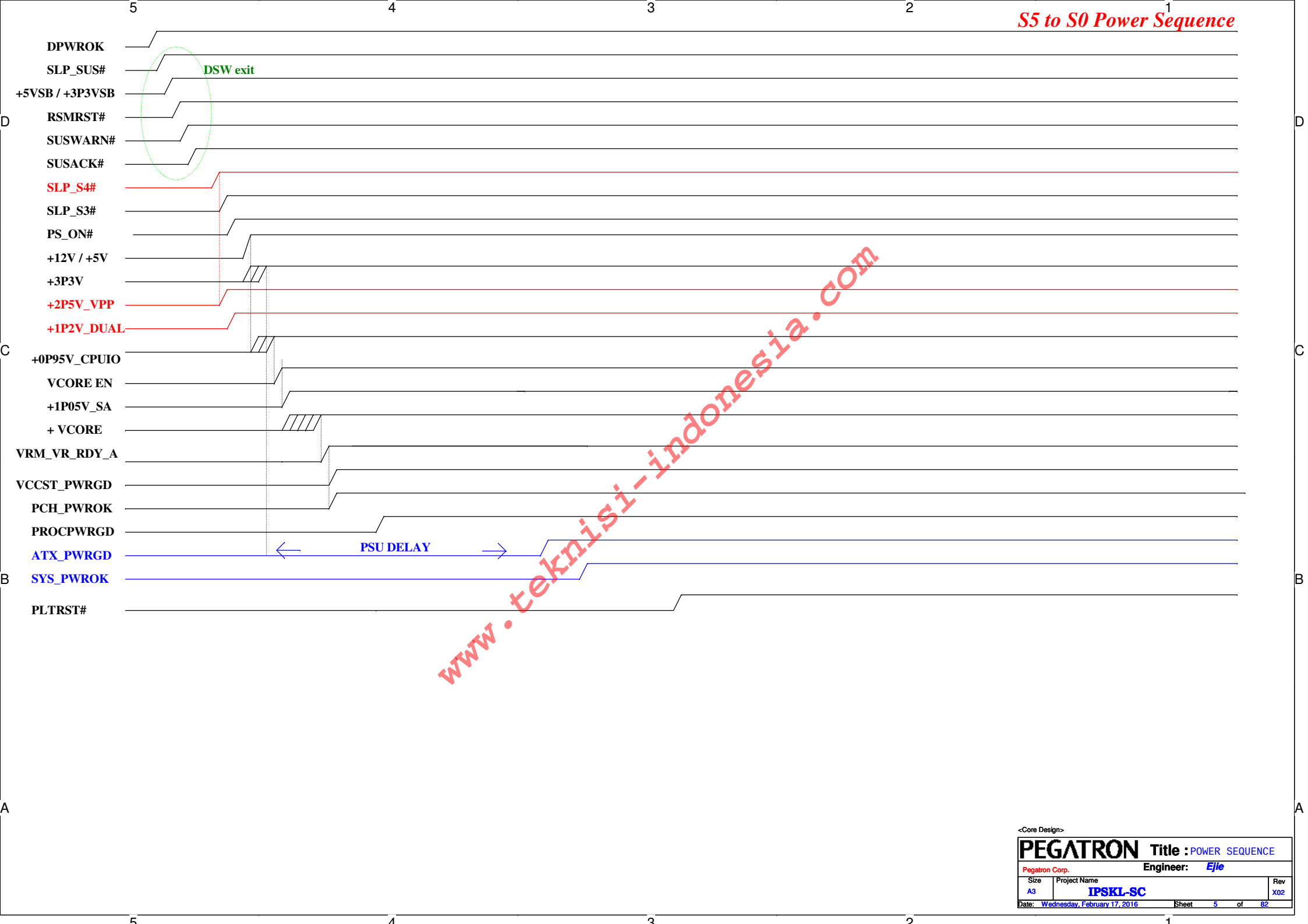


Schematics Change History			
Version	Date	Page	Comments
X00	2015/08/26	45	Add Front USB Conn
X00	2015/08/26	49	EC change to SIO SCH5553-NU
X00	2015/08/26	NA	Remove HDMI
X00	2015/08/26	710	Add USB2.0 X 4
X00	2015/08/26	51	Add HDD LED Conn
X00	2015/08/26	41	LAN chip use QUALCOMM/E2400-RIV1-RL
X00	2015/08/26	74	Add NUT for SSD of 2242
X00	2015/08/26	83	LED Control header change to 12P
X00	2015/08/26	NA	Remove Front panel header
X00	2015/08/26	71	Add TBT header
X00	2015/08/26	310	Type C Conn change to JAE/DX07S024JJ2R1300
X00	2015/08/26	72	FAN power soucer change to +12V_CPU
X00	2015/08/26	38	CC IC change to TI/TPS25810RVC
X00	2015/08/26	39	Add MUX/ASM1542
X00	2015/08/26	53	Add (PR70244) +3VSB S0-G3 discharge impedance
X00	2015/08/26	29	Add cap (F3CB1) for SPI EA overshoot problem
X00	2015/08/26	72	Separate CPU FAN to two Header (CPU & PUMP)
X00	2015/08/26	26	Add GPIO to detect PCH Heatsink
X00	2015/08/26	23	Connect B12 to PCH GPIO for thunderbolt card usage
X00	2015/08/26	76-78	Add 0-Ohm (NI) resistors to SMBus Lines for PCIE X4
X00	2015/08/26	83	Connect LED_I2C, rather than SMBUS
X00	2015/08/27	74	Add cap on H8 & H7
X00	2015/08/28	22	Change SR367 to 620 ohm
X00	2015/08/28	22	Change SR7630 to 2.2 K
X00	2015/08/28	21	Change all Resistance of AZ signal to 22 ohm
X00	2015/08/28	10	Change HR28 to 33 ohm
X00	2015/08/28	20	Change SR116 to 8.2K ohm
X00	2015/08/28	10	Change HR26 to 499 ohm
X00	2015/08/28	45	Change OC# P/U type.
X00	2015/08/28	48	Add 0 ohm on PROCHOT#
X00	2015/08/28	21	Change SR256 to NI
X00	2015/08/28	29	Change HR86 to 0 ohm
X00	2015/08/28	72	FOLLOW SPI topology (single device)
X00	2015/08/31	20	Change LPC signal serial resistance to 0 ohm.
X00	2015/08/31	29	Remove SR7636
X00	2015/08/31	63	Change PR5822 to 75 ohm
X01	2015/09/21	28	NI F3R13 for SLP_S4 fail
X01	2015/09/21	22,11	NI SR653 and OR52 change to 1K ohm for VCCST_PWRGD, PCH_PWROK fail
X01	2015/09/21	68	PQ115 change part to DIODES 3904 ,PR381 change to 1K ohm for VTT no power
X01	2015/09/21	19	Change Board ID resistance For X01
X01	2015/09/21	55	Add reserver 0 ohm PR70297 for S_dual for wake function
X01	2015/09/21	41	Add LAN LED ESD (UD8878,UD8879,UD8880,UD8881)
X01	2015/09/21	70	TBT connector change to 1208-00AJ000
X01	2015/10/15	56	Modify +1V_ST/+1P2V_SUS/+3.3V_SUS for power saving
X01	2015/10/15	11	Remove HR122
X01	2015/10/15	70	Remove not use GPIO GPP_F22/ GPP_F23/ GPP_F10~F14/GPP_A17~A23/ GPP_E11/GPP_G13/GPP_H10~H11/GPP_H13~15
X01	2015/10/15	02	Remove Buzz
X01	2015/10/15	36	Modify usb3.1 circuit on type-a for jitter issue
X01	2015/10/26	43	Change smaller part, Let CE3, CE4 close the front USB
X01	2015/10/26	45	SATA port change , follow customer require
X01	2015/10/26	36	UR69686 change to 12.1K for ASM1142 USB driven
X01	2015/10/26	22	SR659 follow PDG 2.0 change to 470 ohm
X01	2015/10/26	71	for service require, P29,P70 set to black, P461 set to white
X01	2015/10/26	36	UC1 change to 20PF for fine tuing 20M xtal for EA
X01	2015/10/26	40	LC4,LC5 change to 18PF for fine tuing 25M xtal for EA
X01	2015/10/26	48	OR5 change to 20K ohm for EA sequence
X01	2015/10/26	48	OR6 change to 7.68K ohm for EA sequence
X01	2015/10/26	68	PC485 change to NI for EA sequence
X01	2015/10/26	82	ADD AC193~AC196 (100pf cap) for RF requirment
X01	2015/10/26	60	Change PU5 en pin design for EA sequence
X01	2015/10/26	24	Change SR411~Sr412,SR423to shoot pin
X01	2015/11/02	73	Change NUT H7,H8 to S1X00002E167 for EMI and Audio vender solution.
X01	2015/11/02	24	Add SCB10 for EA solution
X01	2015/11/02	20	Add C414~C417 dor LPC EA solution.
X01	2015/11/02	42,44,80	Change UR6,UR69716,UR69718,UR69722 to 51K for OC# Voltage slolution.
X01	2015/11/05	10	SR245 Change 33 ohm to 20 ohm
X02	2015/12/22	19	Change board ID to 0 1 0
X02	2015/12/22	50	SR17 from 100 ohm change to 330 ohm for HDD LED brightness.
X02	2015/12/22	36	UC1 from 20pf change to 18 pf for 20Mhz EA Xtal issue.
X02	2015/12/22	33	XCE14 from change to 10pf for RF issue (power noise EA report is base on the 10pf to measure)
X02	2015/12/22	34	ACES,ACE6 from 22uf MLCC change to 10uf EL cap for Audio quality (Audio report base on this configuration).
X02	2015/12/22	71	FCE1,FCE4,FCE5 from 100uF EL cap change to 22uF MLCC for factory DFM requirment
X02	2015/12/22	41	Reserve the +3P3V_LAN control schematic for WOL ACPI LED behavior.
A00	2016/02/24	48	Delete VRM_Q1,O2C3 for FAN abnormal behavior
A00	2016/02/24	19	SR7696 :I ,SR712:NI , update Board ID from X02(010) to A00(011)
A00	2016/02/24	58	completed power test, change to short on PR6606,PU641,PU642
A00	2016/02/24	36	UC1 from 18pf change to 15 pf for EA 20Mhz Xtal issue.
CHANGE HISTORY			
©Gee Design			
PEGATRON		Title :	
Project Code		Engineer: Epe	
Rev	Project Name	Date	
001	TPSRL-BC	2016-02-24	
Rev	Rev	Rev	Rev





S5 to S0 Power Sequence



<Core Design>

PEGATRON		Title : POWER SEQUENCE	
Pegatron Corp.		Engineer: Ejle	
Size	Project Name	Rev	
A3	IPSKL-SC	X02	
Date: Wednesday, February 17, 2016		Sheet	5 of 82

	CPU Skylake-S 42 K-SKU
+VCORE	-> 100A (Imax)
+0P95V_CPUIO	-> 5.5A (Imax)
+1P05V_SA	-> 11.1A (Imax)
+V_AXG	-> 45A (Imax)

	PCH
+1VSB	-> 7.858A
+3P3V	-> 0.007A
+3P3VSB	-> 0.78A
+3P3VA	-> 0.20A
+BATT	RTC(G3) -> 6uA

	DDR4-2400(4) & Termination
+1P2V_DUAL	-> 10.8A
+VPP(2.5V)	-> 1.12A
+VTT_DDR(0.75V)	-> 0.53A

	PCI Express x 16 (75W)
+12V	-> 5.5A
+3P3V	-> 3.0A
+3P3VSB	WAKE -> 0.375A No WAKE-> 20mA

	PCI Express x 4 (25W)
+12V	-> 2.0A
+3P3V	-> 1.0A
+3P3VSB	WAKE -> 0.375A - 1.24W No WAKE-> 20mA - 66mW

	PCI Express x 4 (25W)
+12V	-> 2.0A
+3P3V	-> 1.0A
+3P3VSB	WAKE -> 0.375A - 1.24W No WAKE-> 20mA - 66mW

	PCI Express x 16 (75W)
+12V	-> 5.5A
+3P3V	-> 3.0A
+3P3VSB	WAKE -> 0.375A No WAKE-> 20mA

	REAR USB2.0 6 PORTS
+5V_DUAL	->3A

	REAR USB3.0 4 PORTS
+5V_DUAL	->4.5A

	M.2 SSD / M.2 WIFI
+3P3V	-> 0.9A / 0.6A

	Killer E2400
+3P3VSB	-> 0.151A

	REAR TYPE C
+5V_DUAL	->3A

	TOP FAN
+12V_CPU	-> 0.8A

	PUMP/CPU FAN
+12V_CPU	-> 0.208A / 0.7A

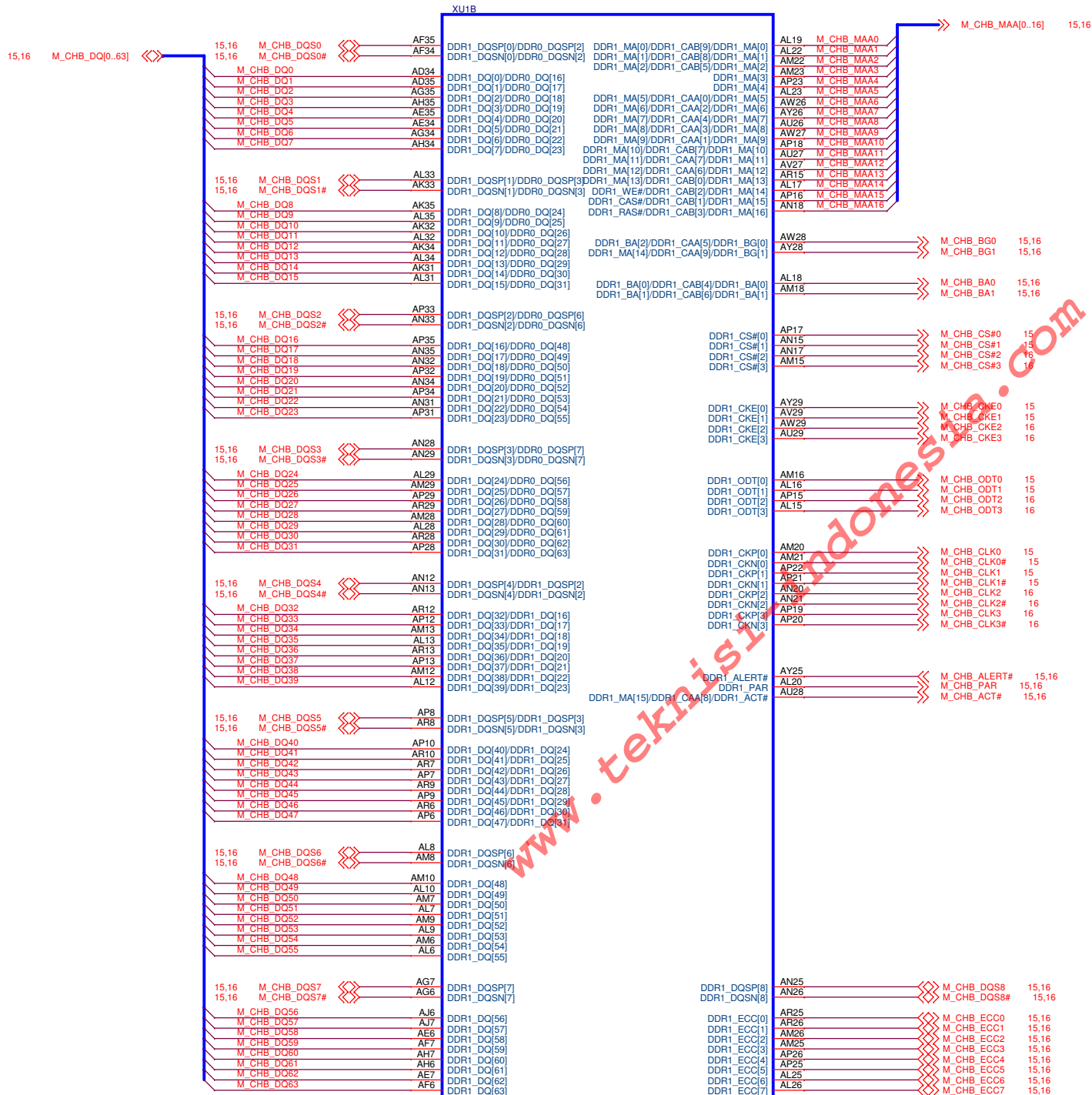
	GFX FAN
+12V_CPU	-> 0.8A

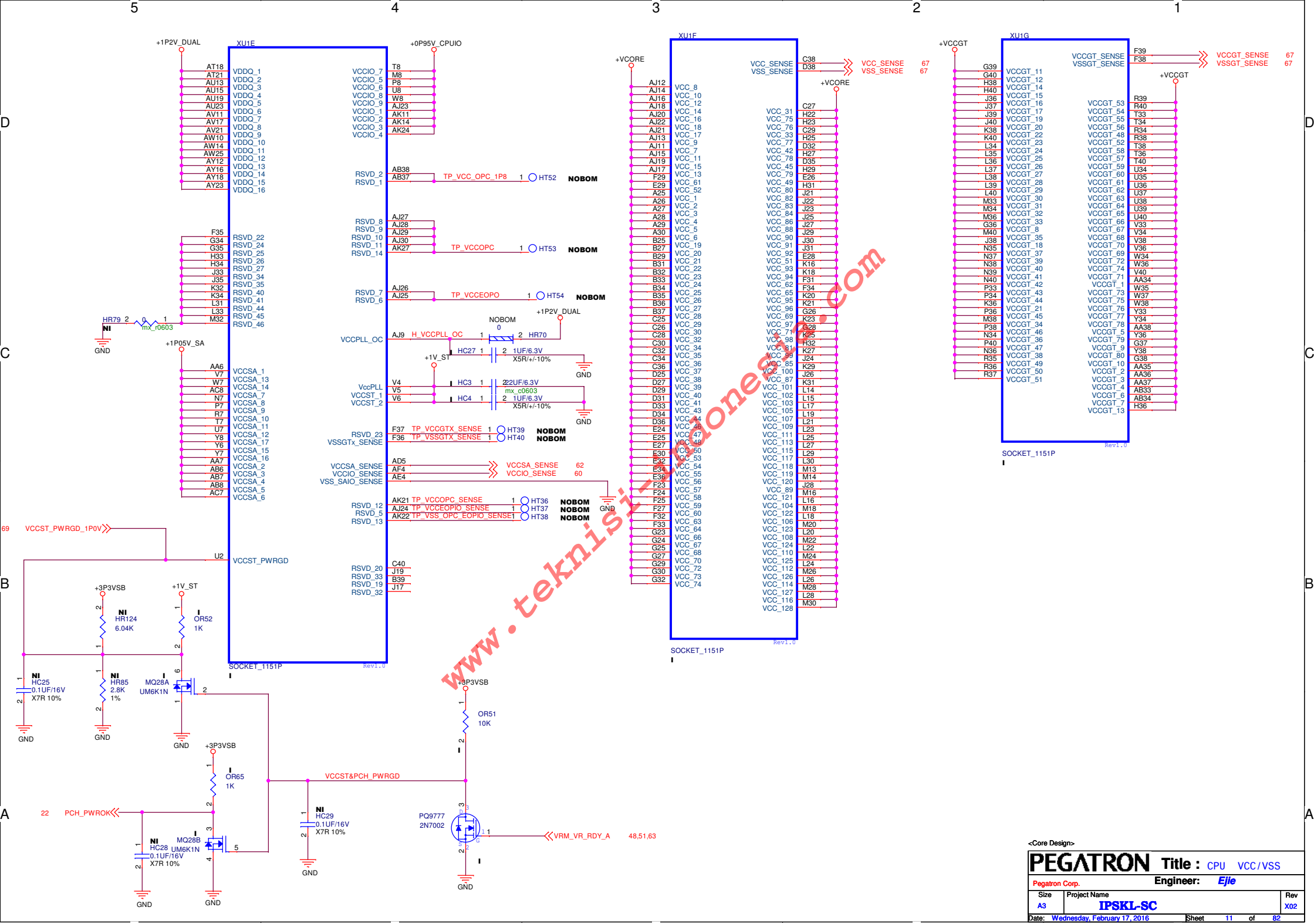
	FRONT USB3.0 2 PORTS
+5V_DUAL	->1A

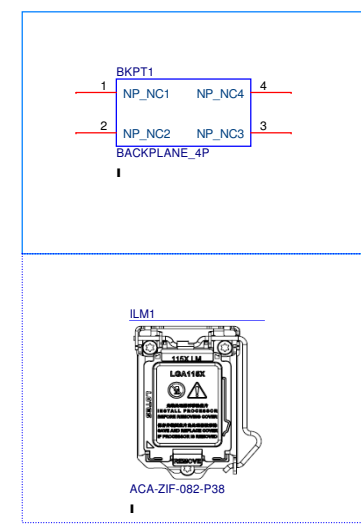
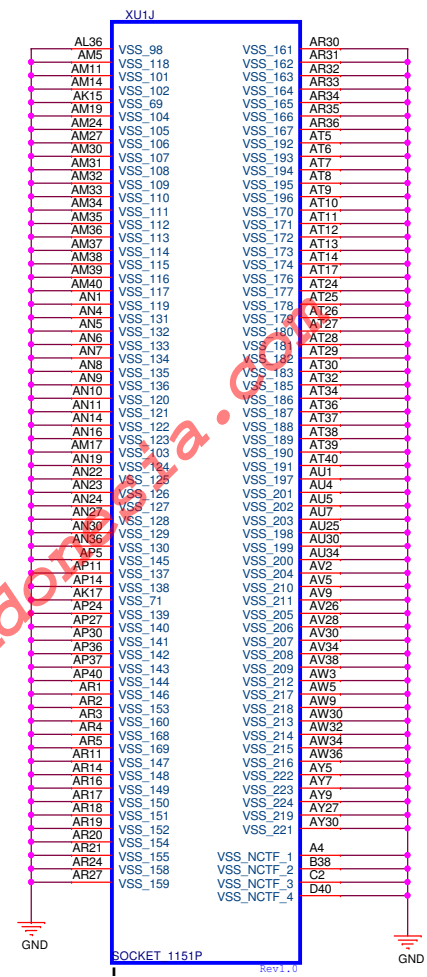
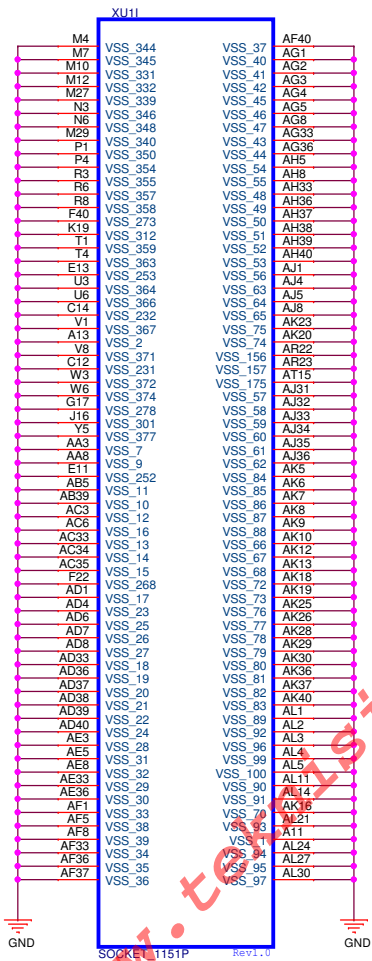
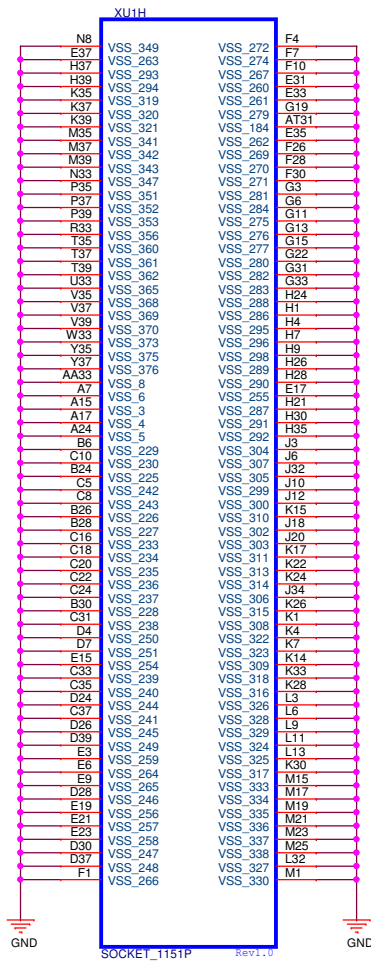
	FRONT USB3.0 2 PORTS Charge
+5V_1VSB_IN	->2.8A

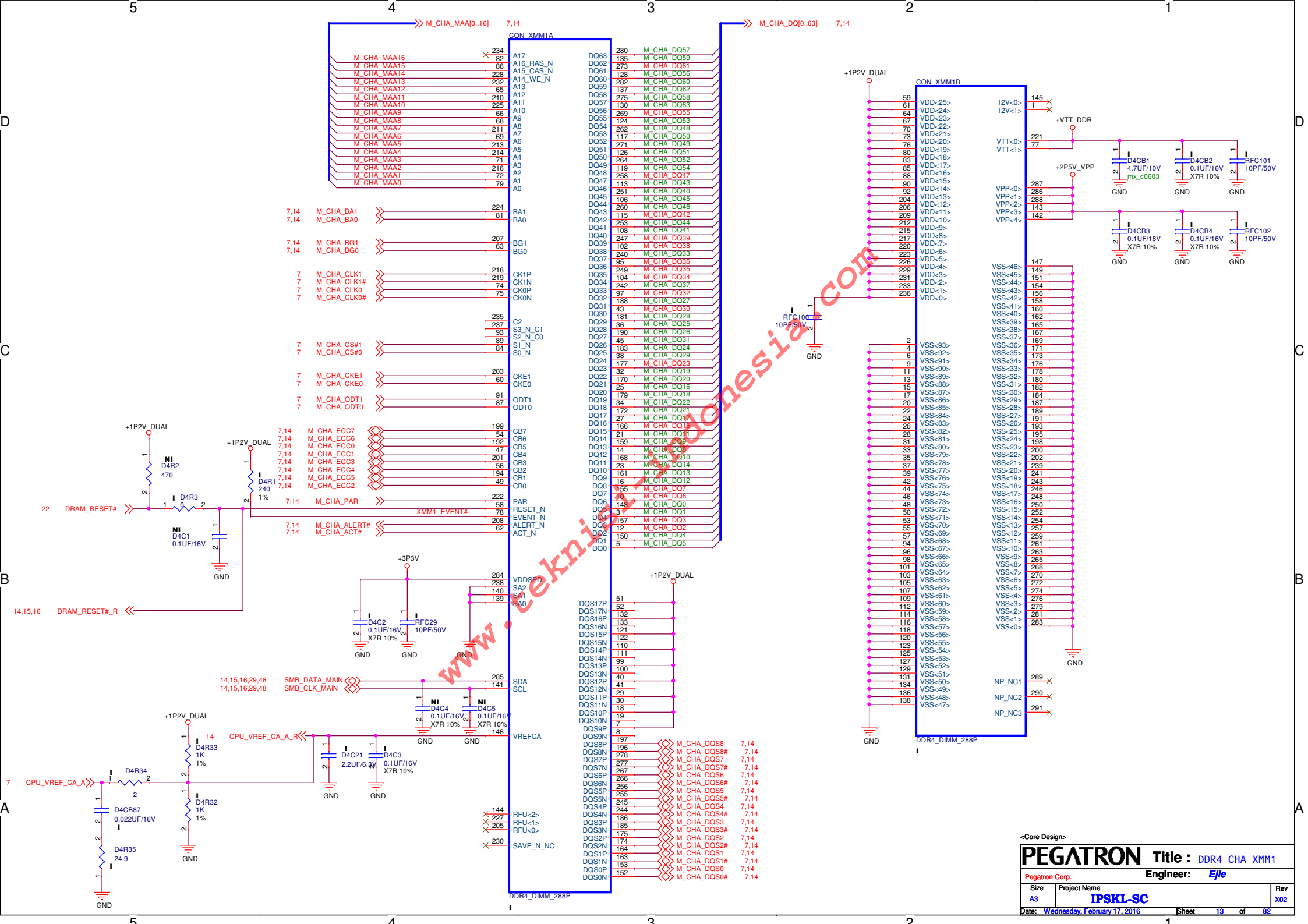
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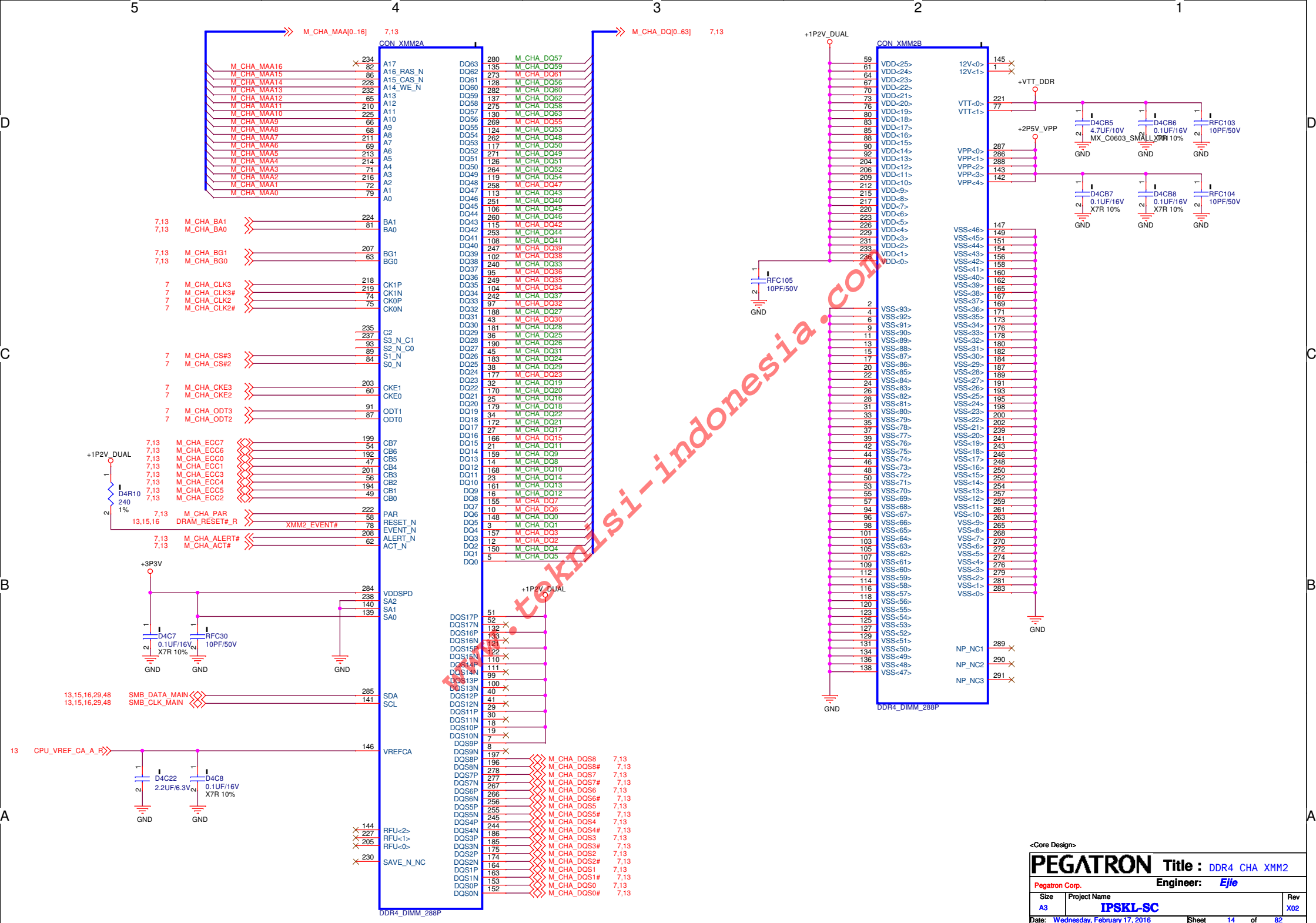
PEGATRON		Title : POWER DISTRIBUTION	
Pegatron Corp.		Engineer: Ejie	
Size A3	Project Name IPSKL-SC	Rev X02	
Date: Wednesday, February 17, 2016		Sheet 6 of 82	

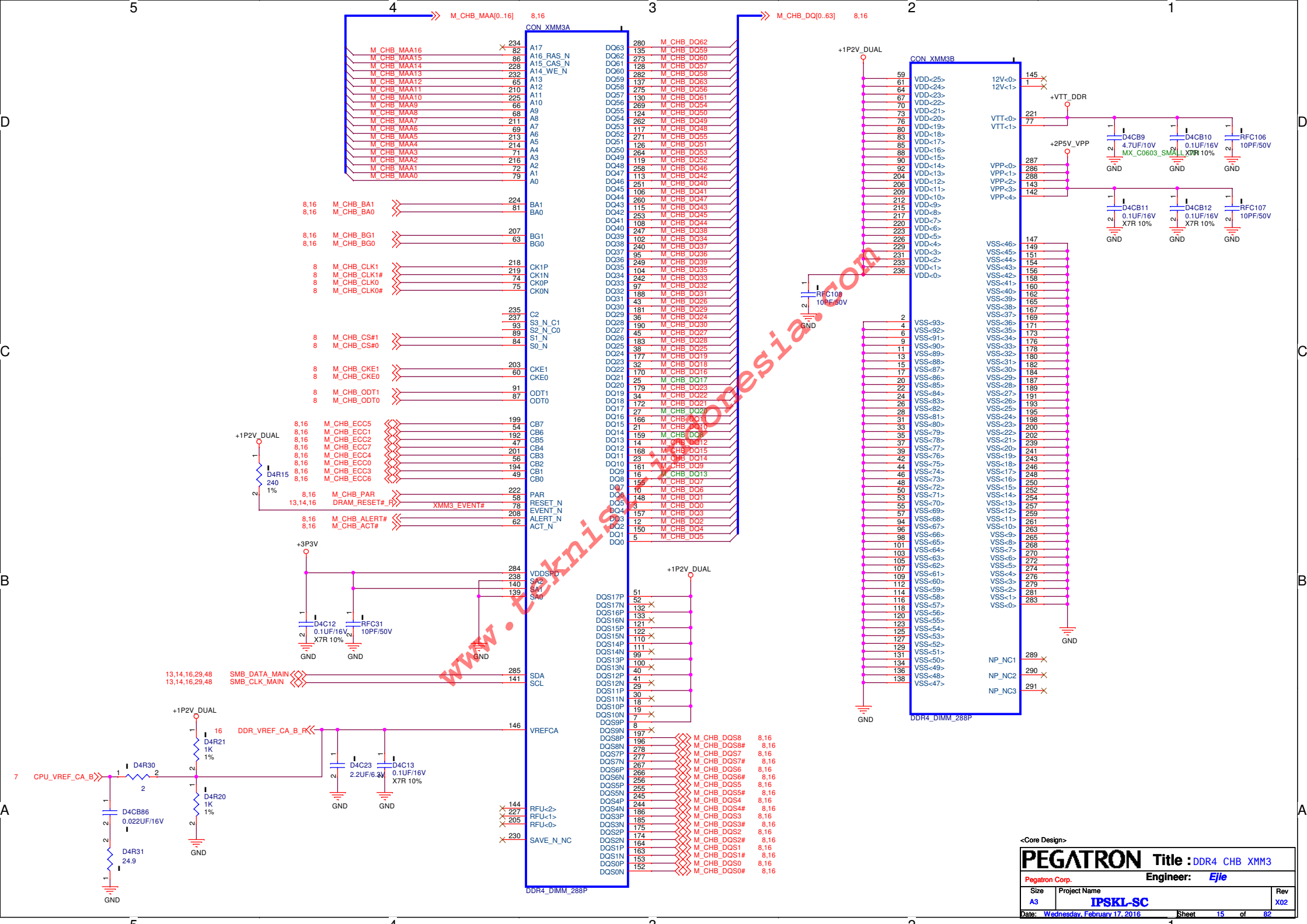


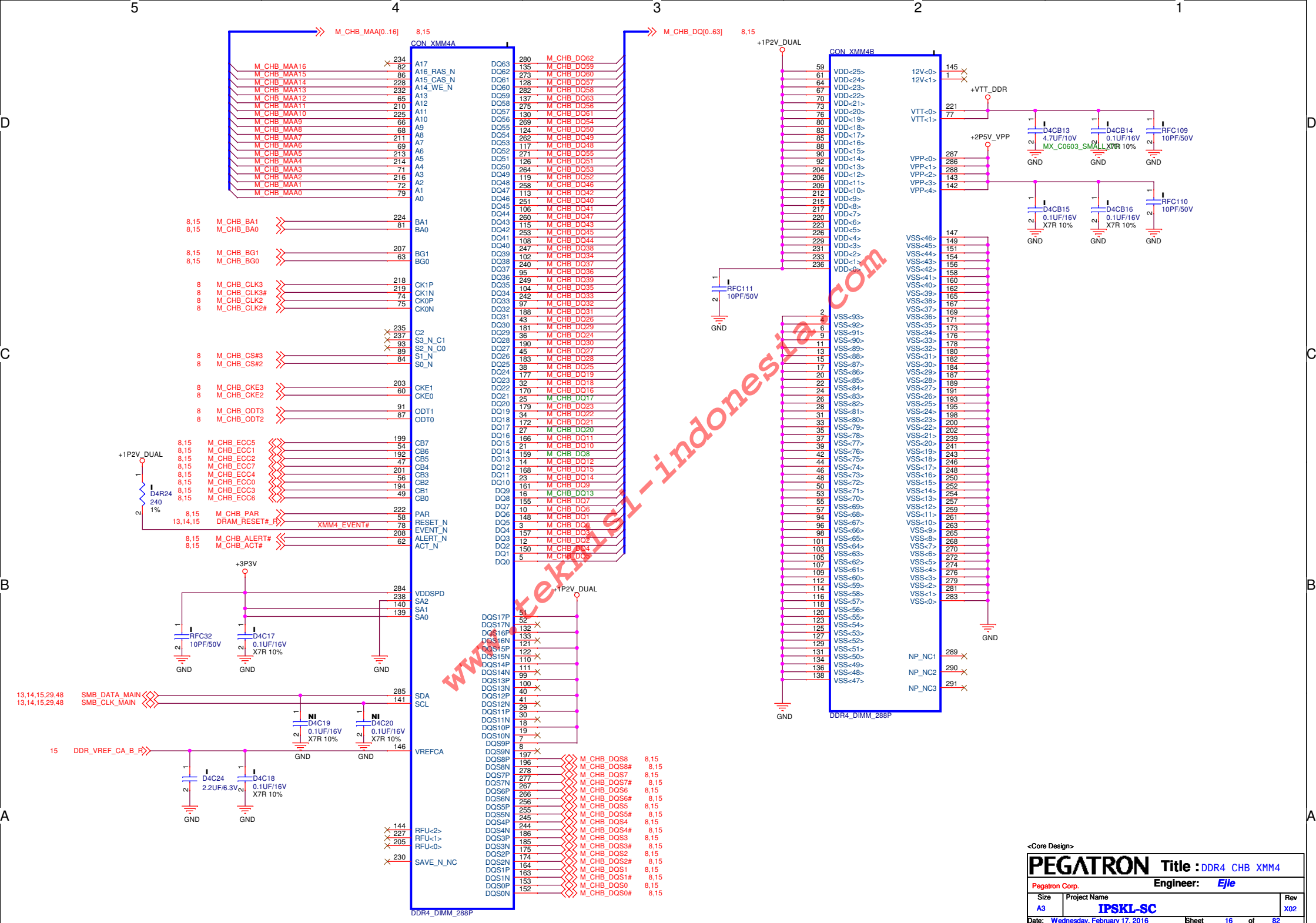








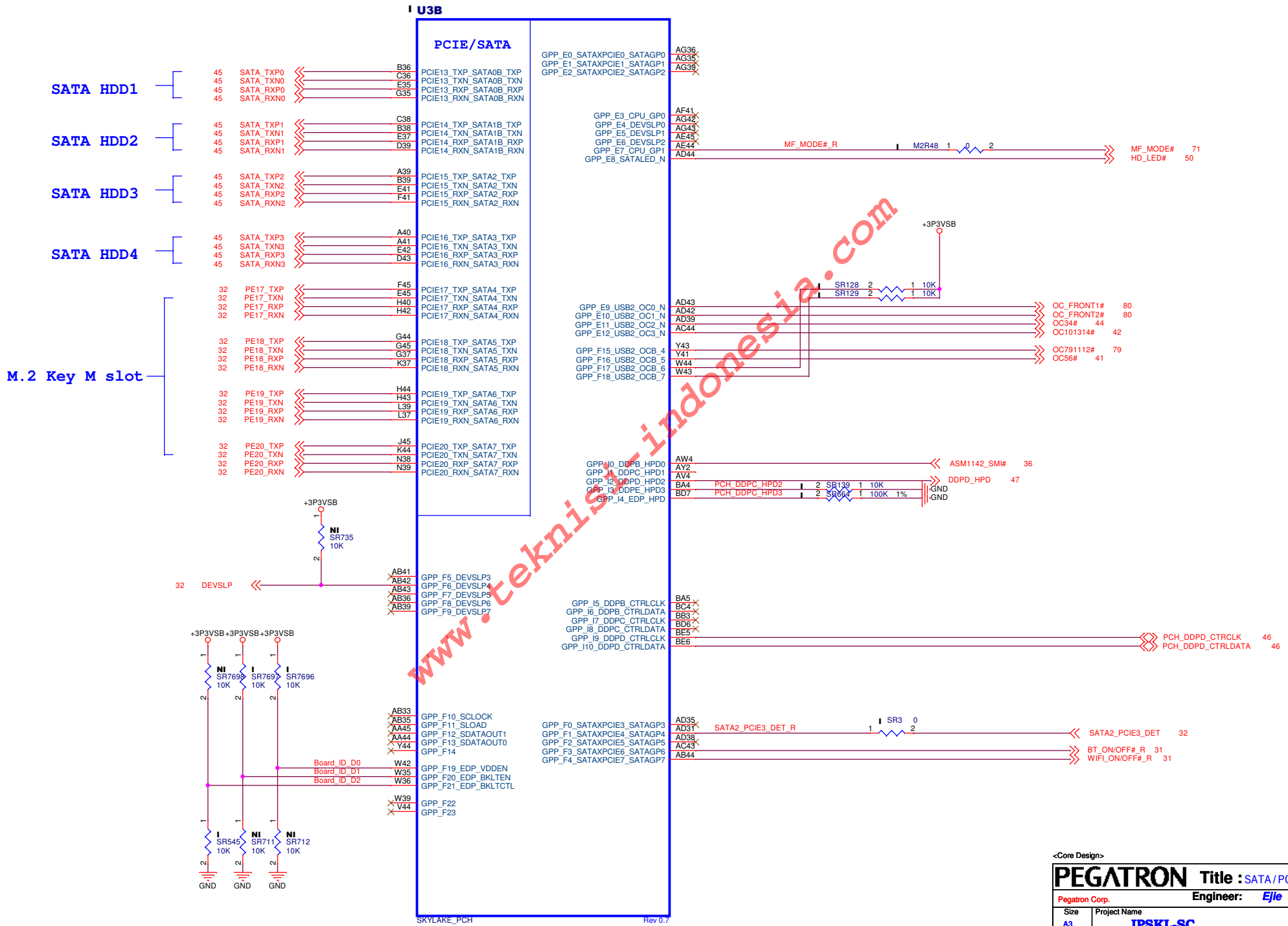


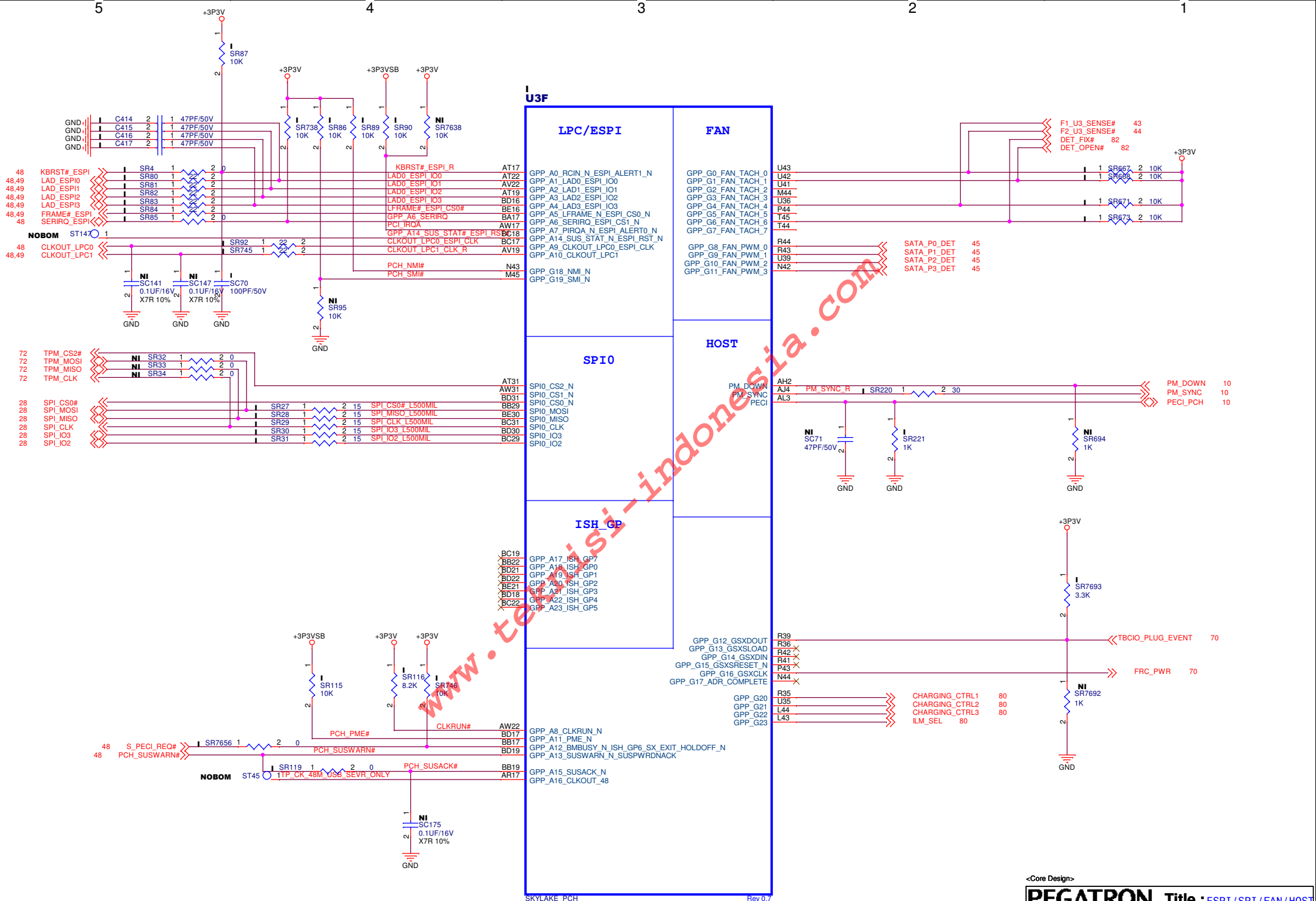


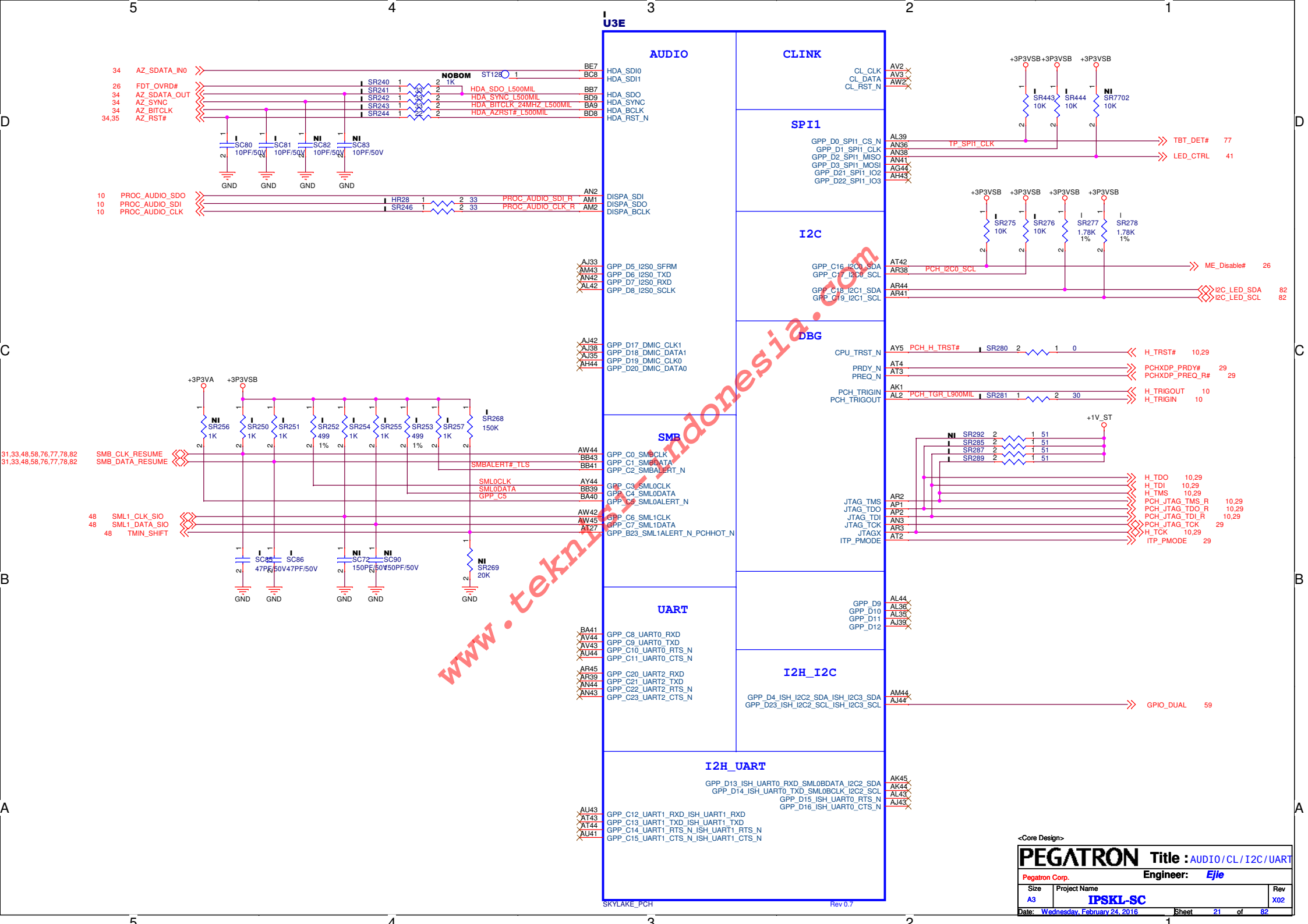


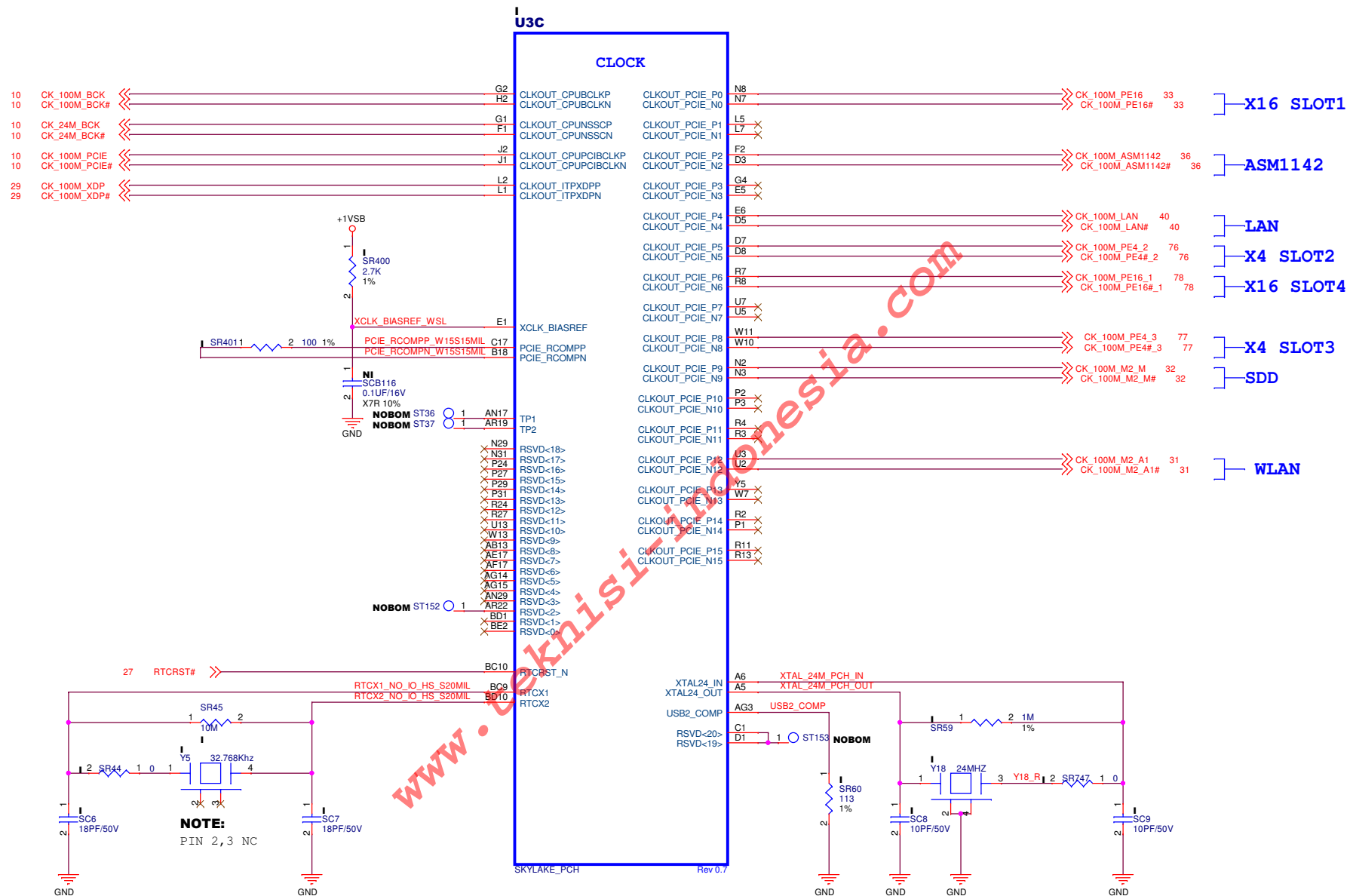
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PEGATRON		Title :DDR4 Termination	
Pegatron Corp.		Engineer: Ejie	
Size A3	Project Name IPSKL-SC		Rev X02
Date: Wednesday, February 17, 2016		Sheet 17 of 82	

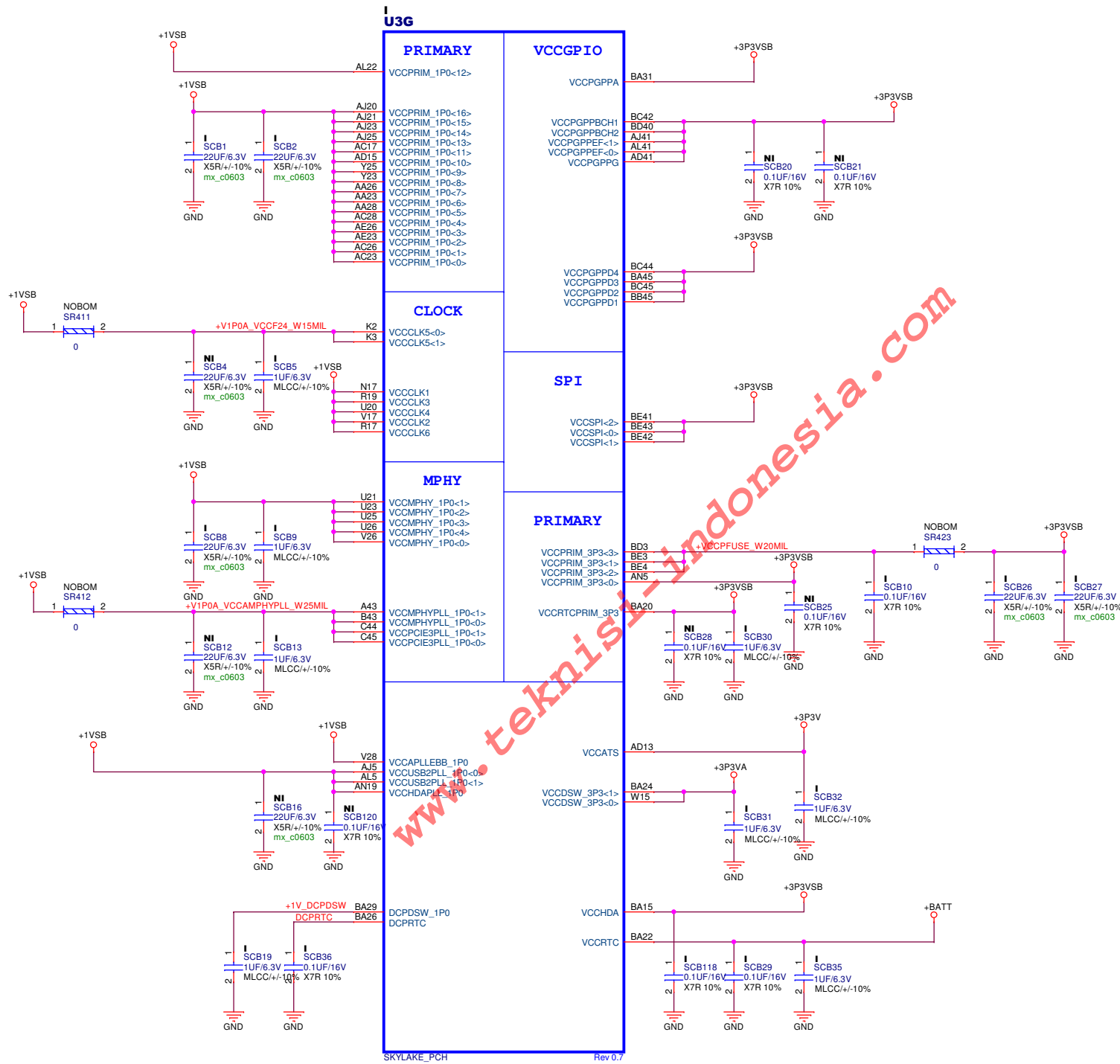


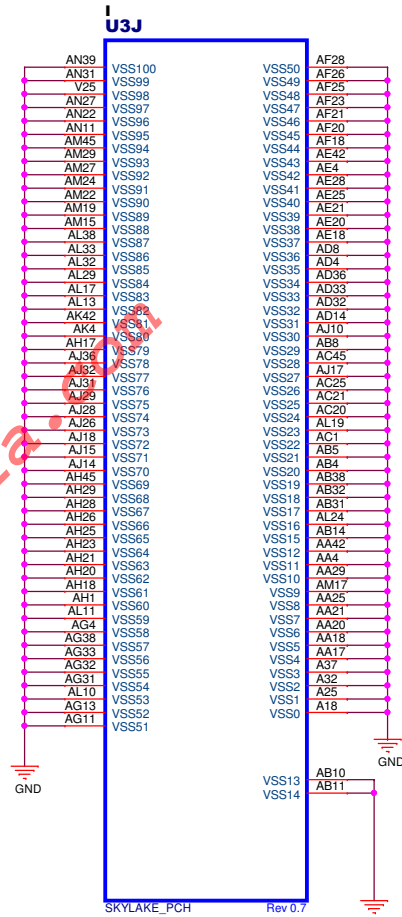
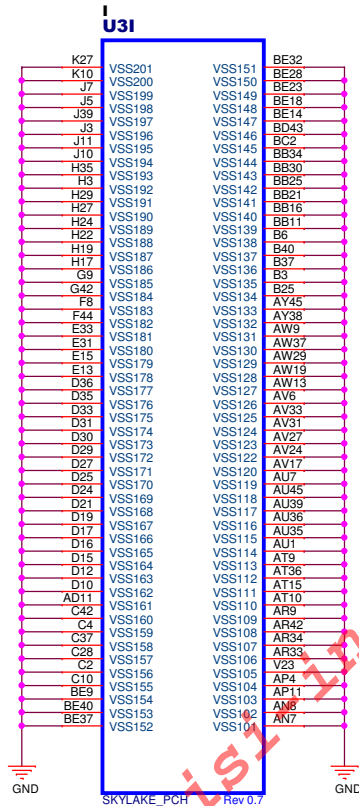
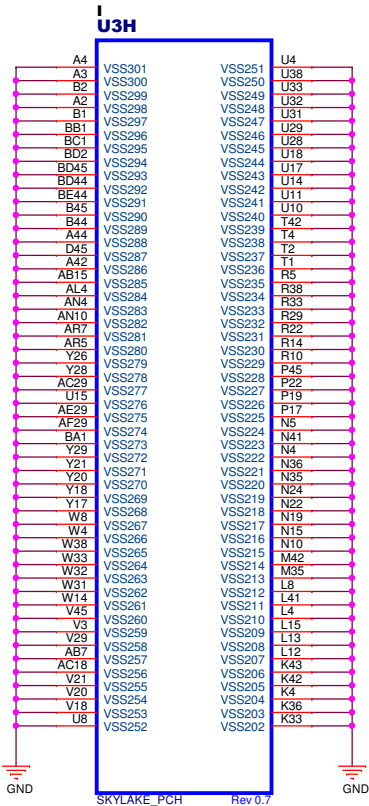




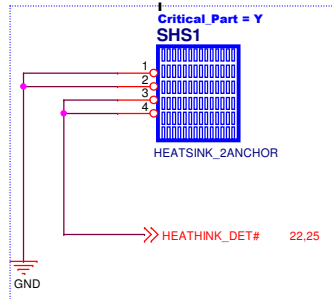


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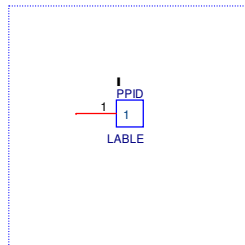




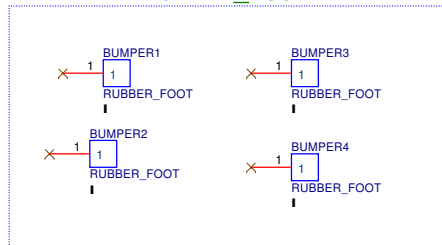
PCH Heatsinker



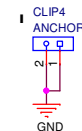
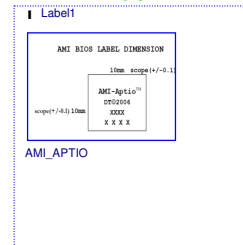
DELL PPID



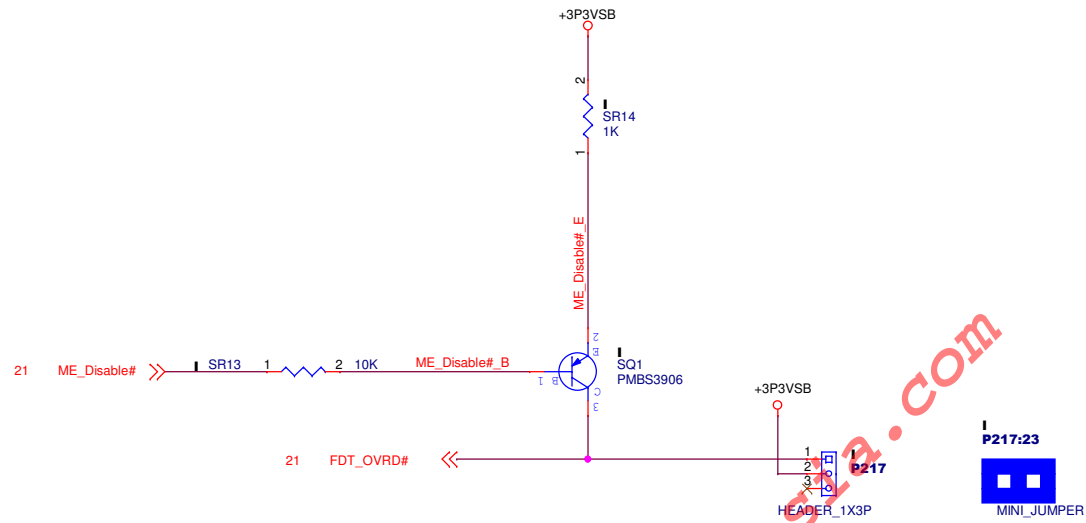
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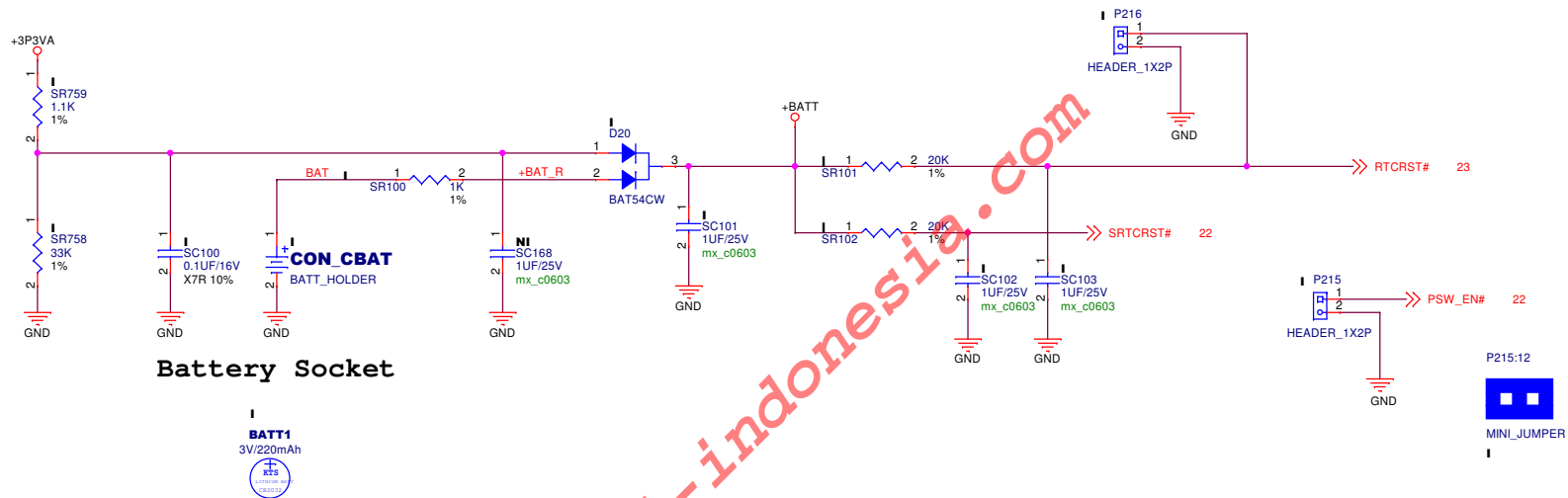
AMI BIOS LABEL



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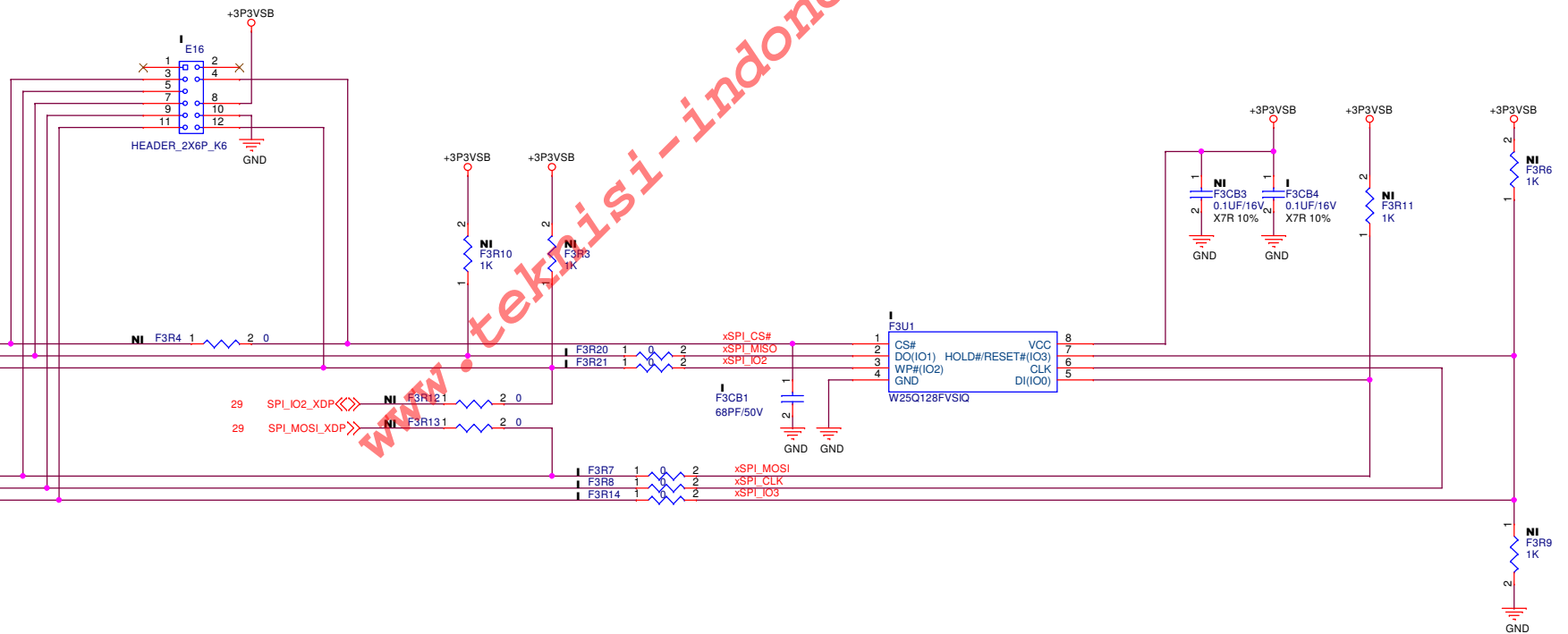


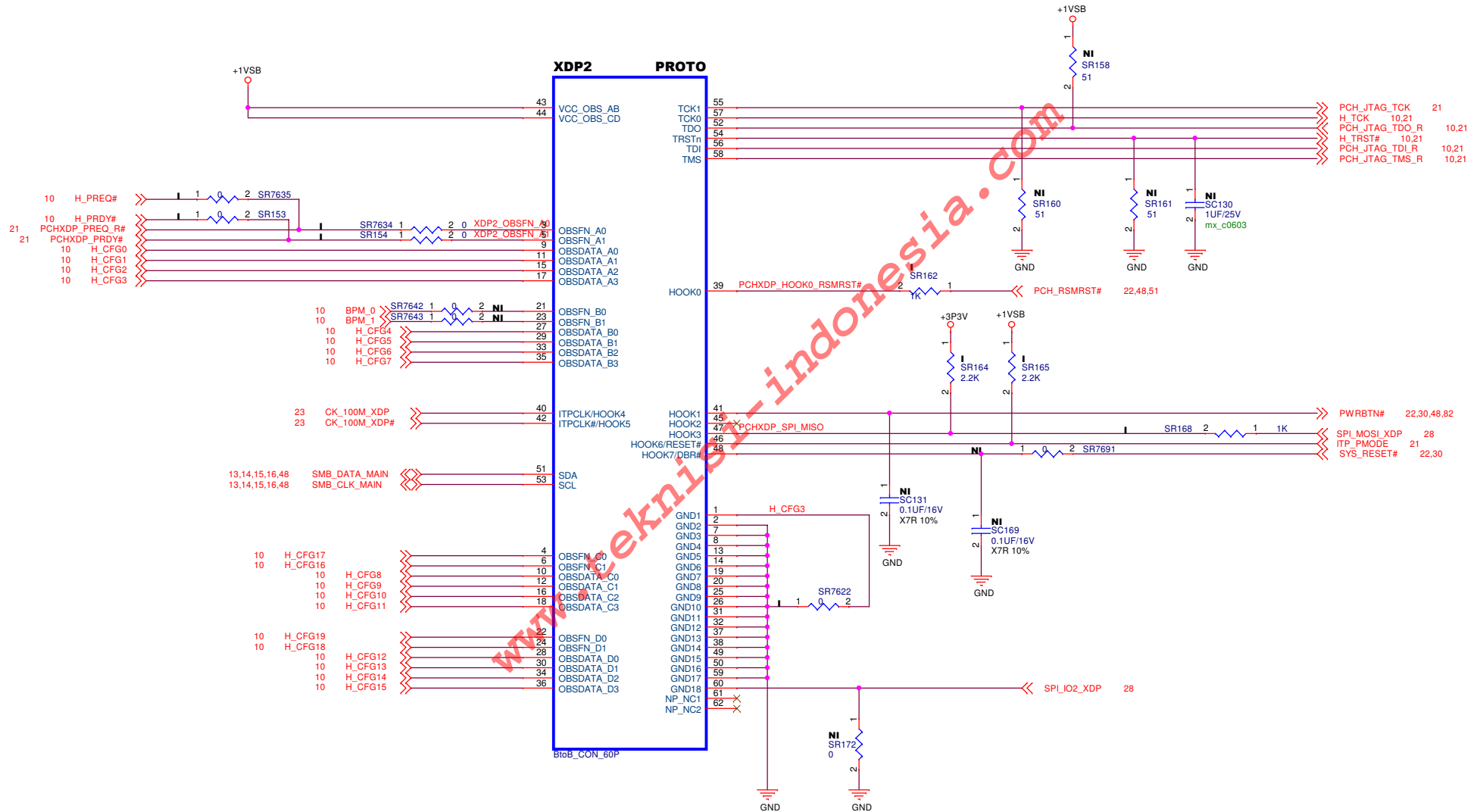
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PEGATRON		Title : PCH_PLTRST	
Pegatron Corp.		Engineer: Ejle	
Size B	Project Name IPSKL-SC		Rev X02
Date: Wednesday, February 17, 2016		Sheet 26 of 82	



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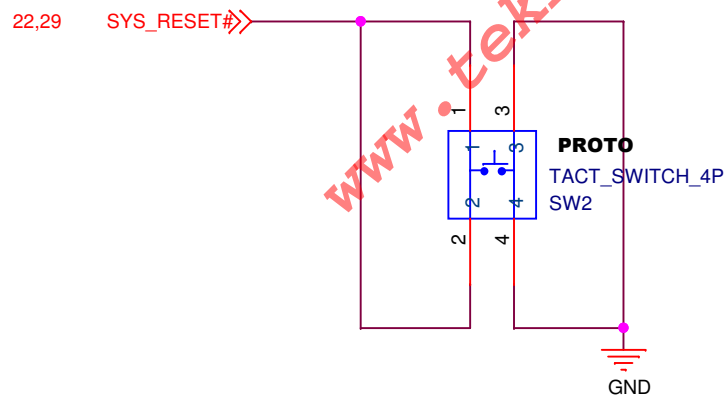
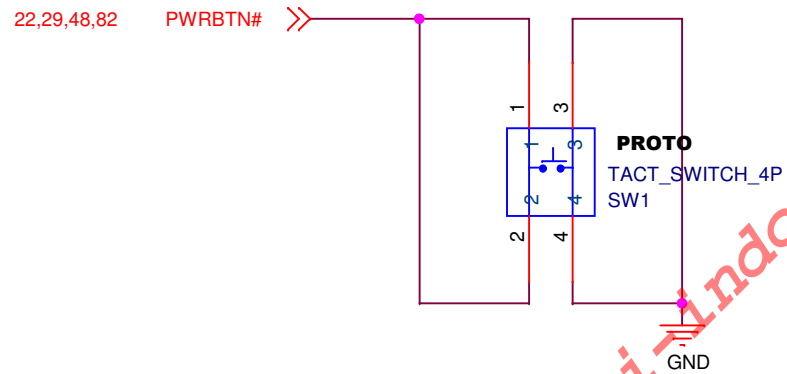
PEGATRON		Title : RTC/CMOS	
Pegatron Corp.		Engineer: Ej/e	
Size A3	Project Name IPSKL-SC	Rev X02	
Date: Wednesday, February 17, 2016		Sheet 27 of 82	





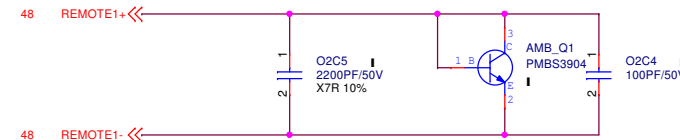
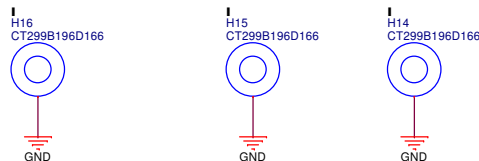
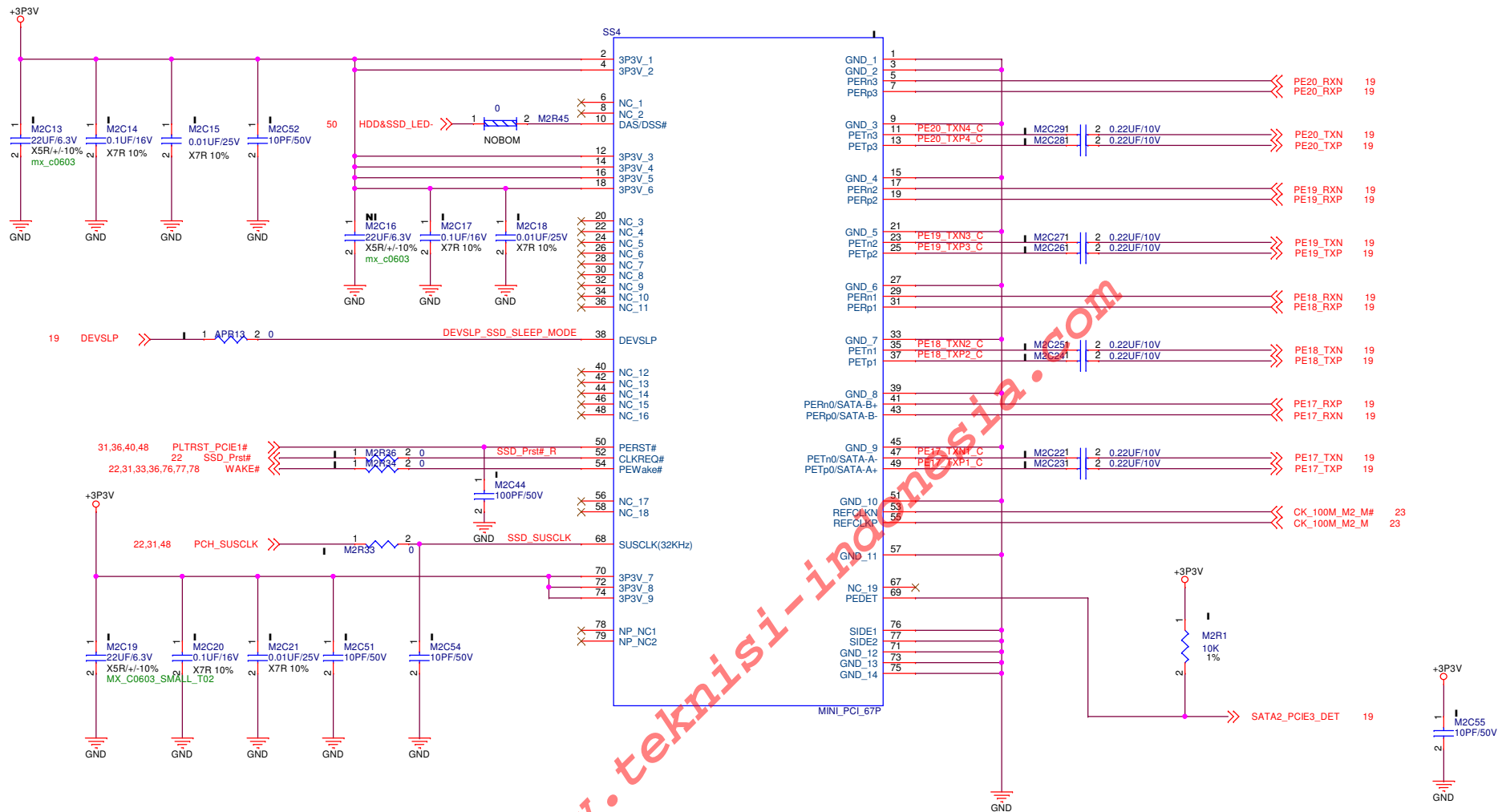
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PEGATRON		Title : XDP	
Pegatron Corp.		Engineer: Ejie	
Size	Project Name	Rev	
A3	IPSKL-SC	X02	
Date: Friday, February 26, 2016		Sheet 29 of 82	



<Core Design>

Title		
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Size	Document Number	Rev
A	<Doc>	<Rev Code>
Date:	Wednesday, February 17, 2016	Sheet 30 of 82



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PEGATRON Title : M.2 KEY M SSD

Pegatron Corp.

Engineer: *Ejle*

Size Project Name

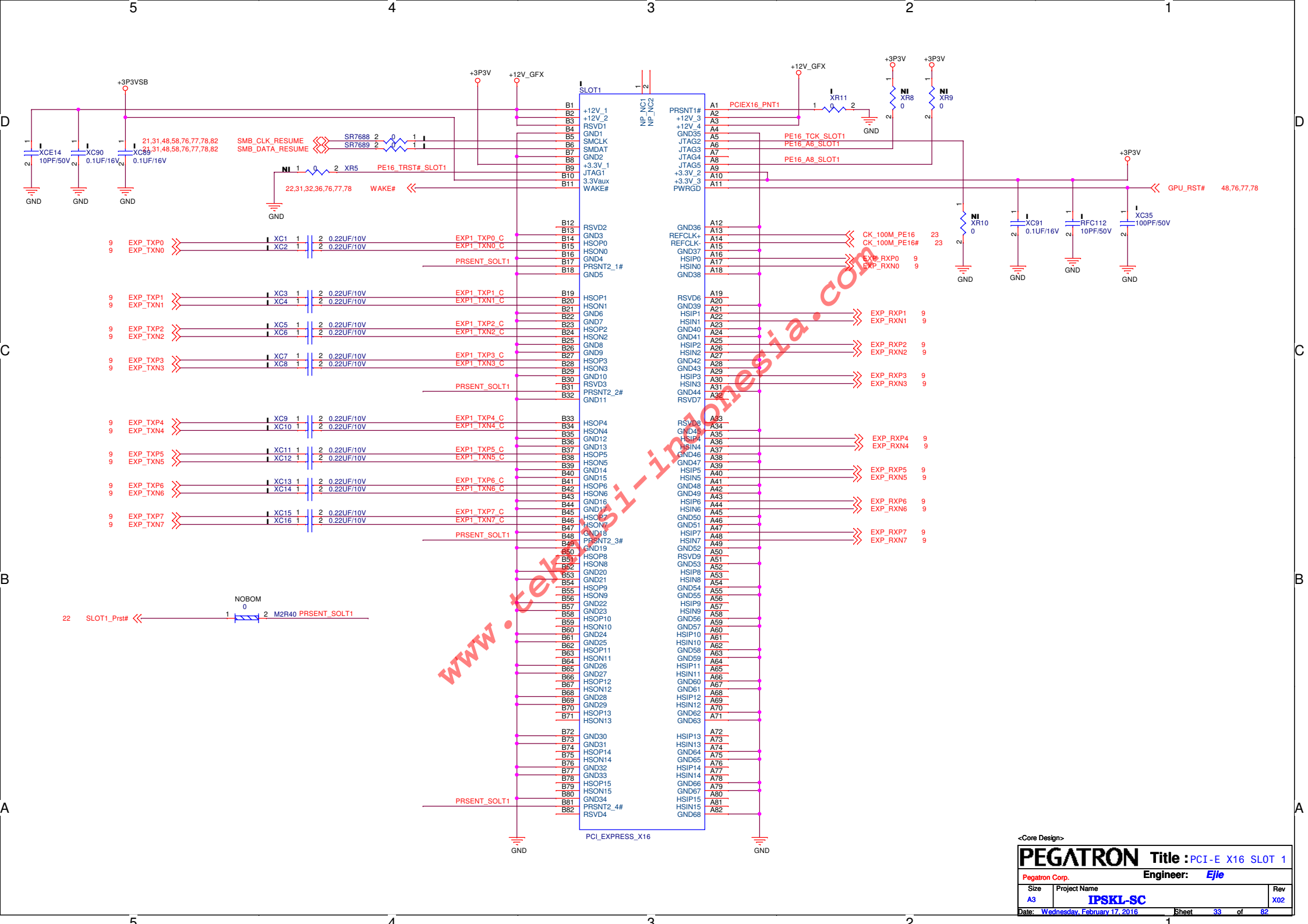
A3 **IPSKL-SC**

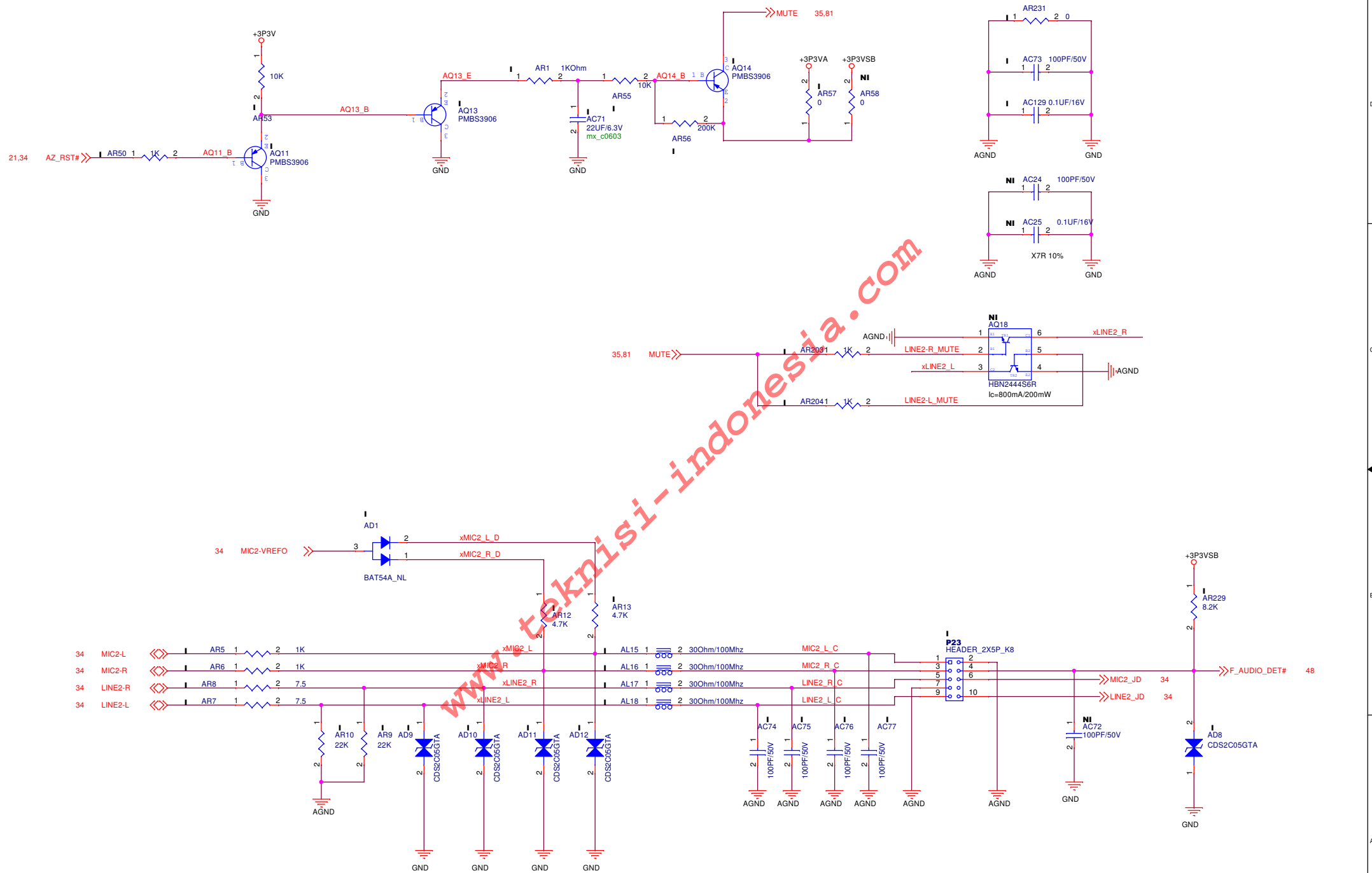
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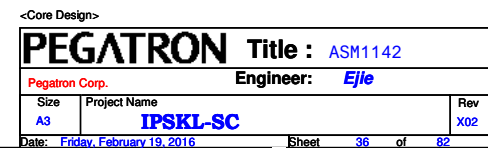
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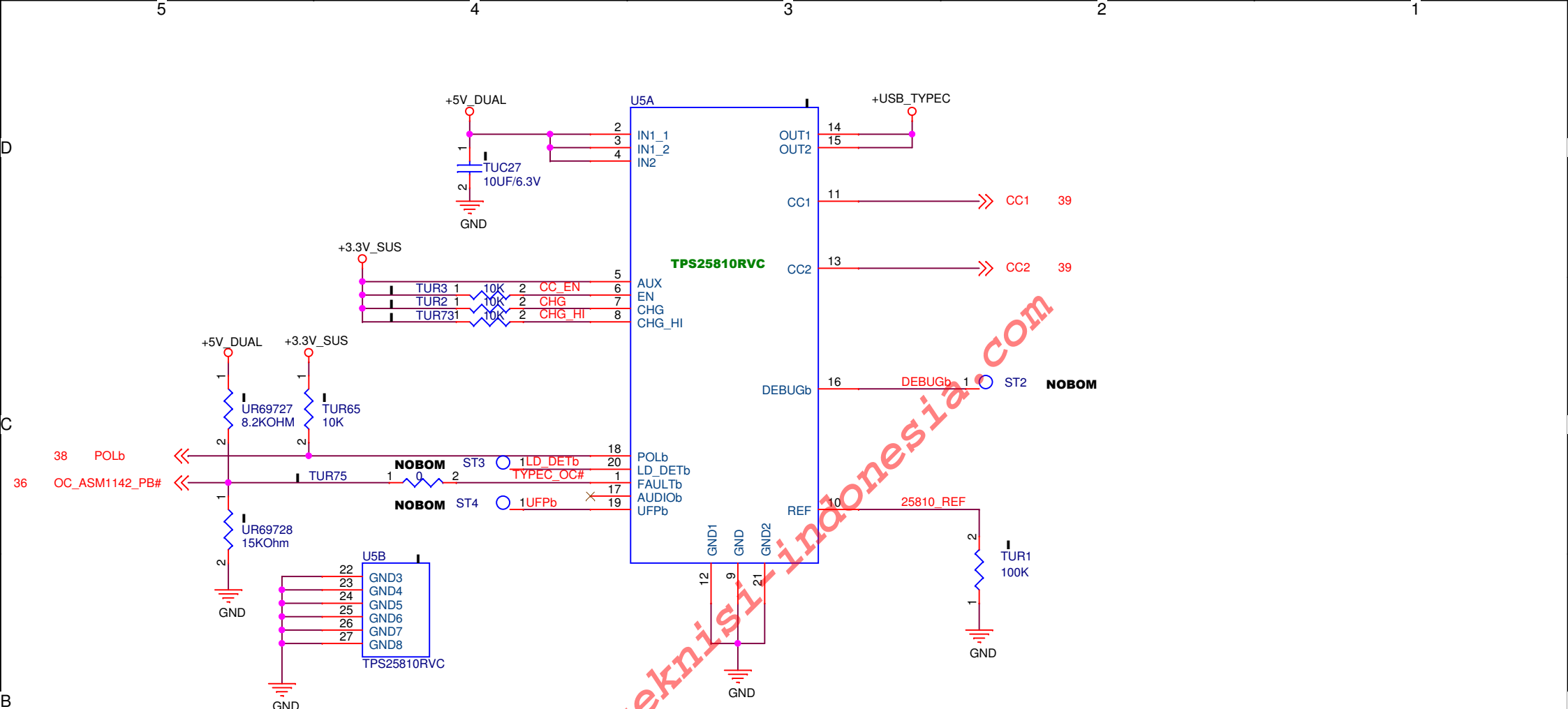
Date: Friday, February 19, 2016

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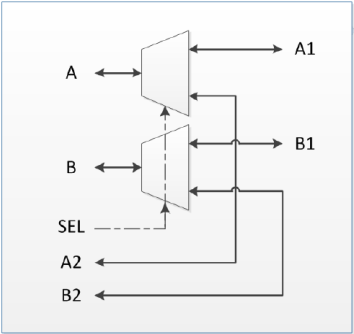
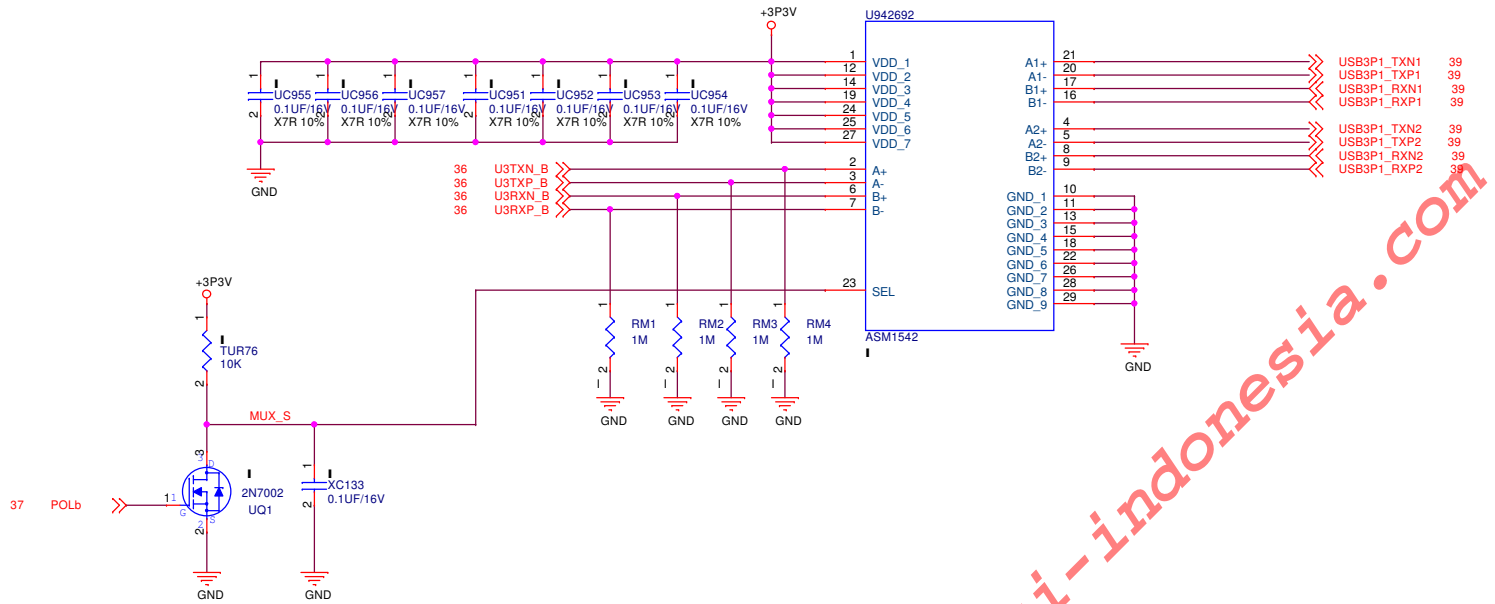






TPS25810 Port	TPS25810 Response							
	CC1	CC2	OUT	VCONN On CC1 or CC2	POLb	UFPb	AUDIOb	DEBUGb
Nothing Attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UFP Connected	Rd	OPEN	IN1	NO	Hi-Z	LOW	Hi-Z	Hi-Z
UFP Connected	OPEN	Rd	IN1	NO	LOW	LOW	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	OPEN	Ra	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	Ra	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Rd	Ra	IN1	CC2	Hi-Z	LOW	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Ra	Rd	IN1	CC1	LOW	LOW	Hi-Z	Hi-Z
Debug Accessory Connected	Rd	Rd	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	LOW
Audio Adapter Accessory Connected	Ra	Ra	OPEN	NO	Hi-Z	Hi-Z	LOW	Hi-Z

CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A



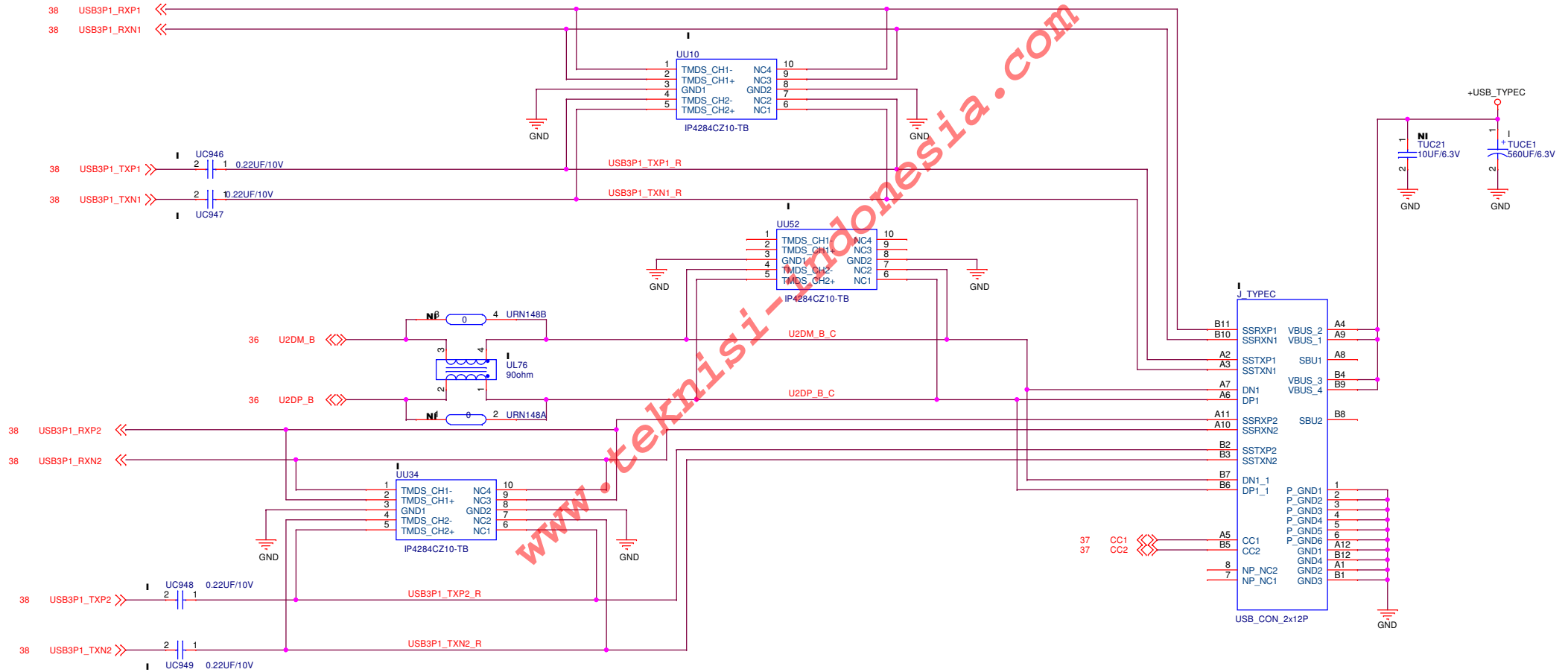
SEL	Function
L	A to A1 & B to B1
H	A to A2 & B to B2

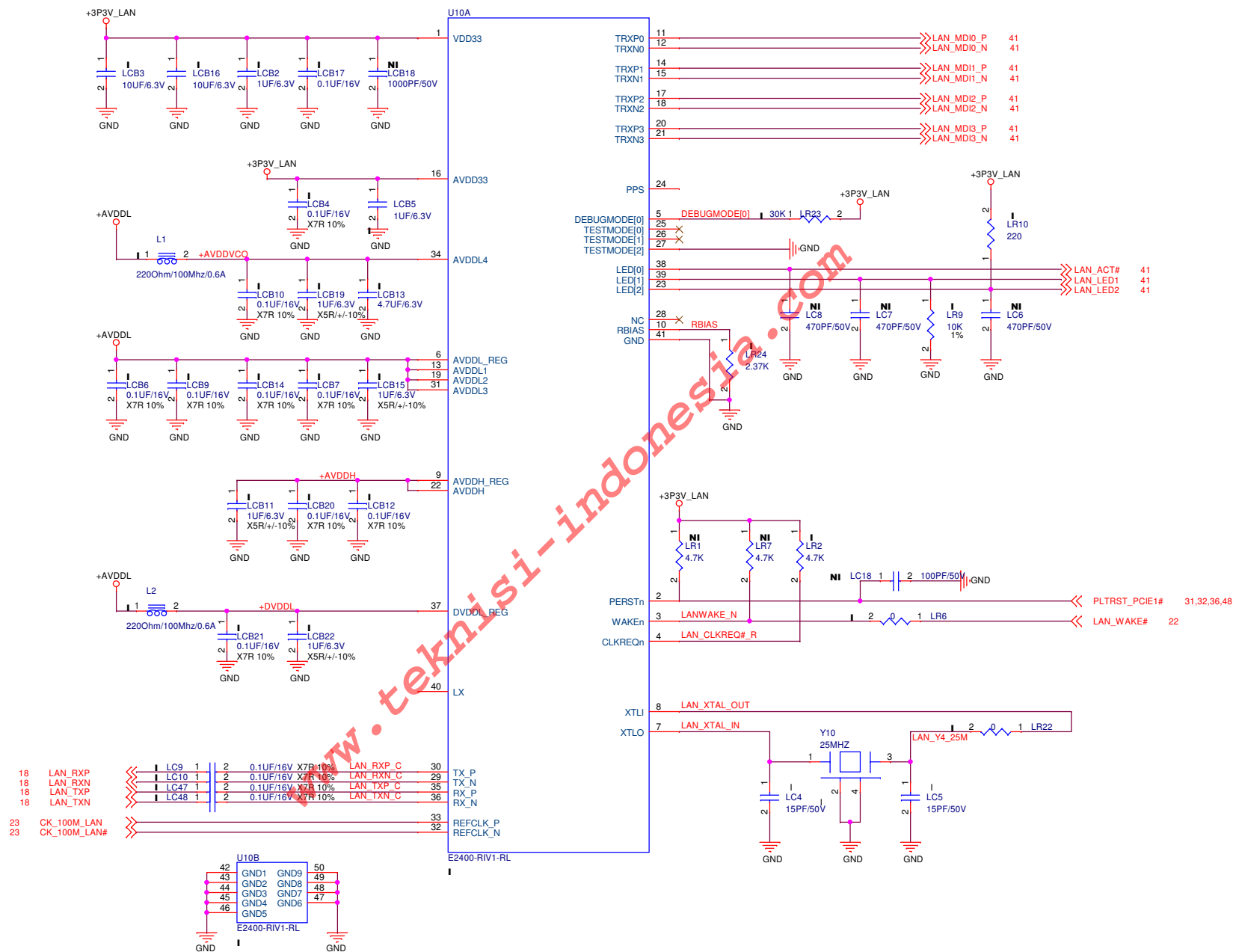
The diagram shows two USB3P1_TXP1_R and USB3P1_TXN1_R signals connected to two IP4284CZ10-TB components. The components are labeled UU10 and UU52. The connections are as follows:

- UU10 (IP4284CZ10-TB):**
 - Pin 1: TMSD_CH1- (connected to USB3P1_TXP1_R)
 - Pin 2: TMSD_CH1+ (connected to USB3P1_TXN1_R)
 - Pin 3: GND1
 - Pin 4: TMSD_CH2- (connected to USB3P1_TXP1_R)
 - Pin 5: TMSD_CH2+ (connected to USB3P1_TXN1_R)
 - Pin 10: NC4
 - Pin 9: NC3
 - Pin 8: GND2
 - Pin 7: NC2
 - Pin 6: NC1
- UU52 (IP4284CZ10-TB):**
 - Pin 1: TMSD_CH1- (connected to USB3P1_TXP1_R)
 - Pin 2: TMSD_CH1+ (connected to USB3P1_TXN1_R)
 - Pin 3: GND1
 - Pin 4: TMSD_CH2- (connected to USB3P1_TXP1_R)
 - Pin 5: TMSD_CH2+ (connected to USB3P1_TXN1_R)
 - Pin 10: NC4
 - Pin 9: NC3
 - Pin 8: GND2
 - Pin 7: NC2
 - Pin 6: NC1

The diagram also shows other components like UL76, UL148A, and UL148B, and signals like U2DM_B_C and U2DP_B_C. A large watermark 'www.teknisi-indonesia.com' is visible across the diagram.

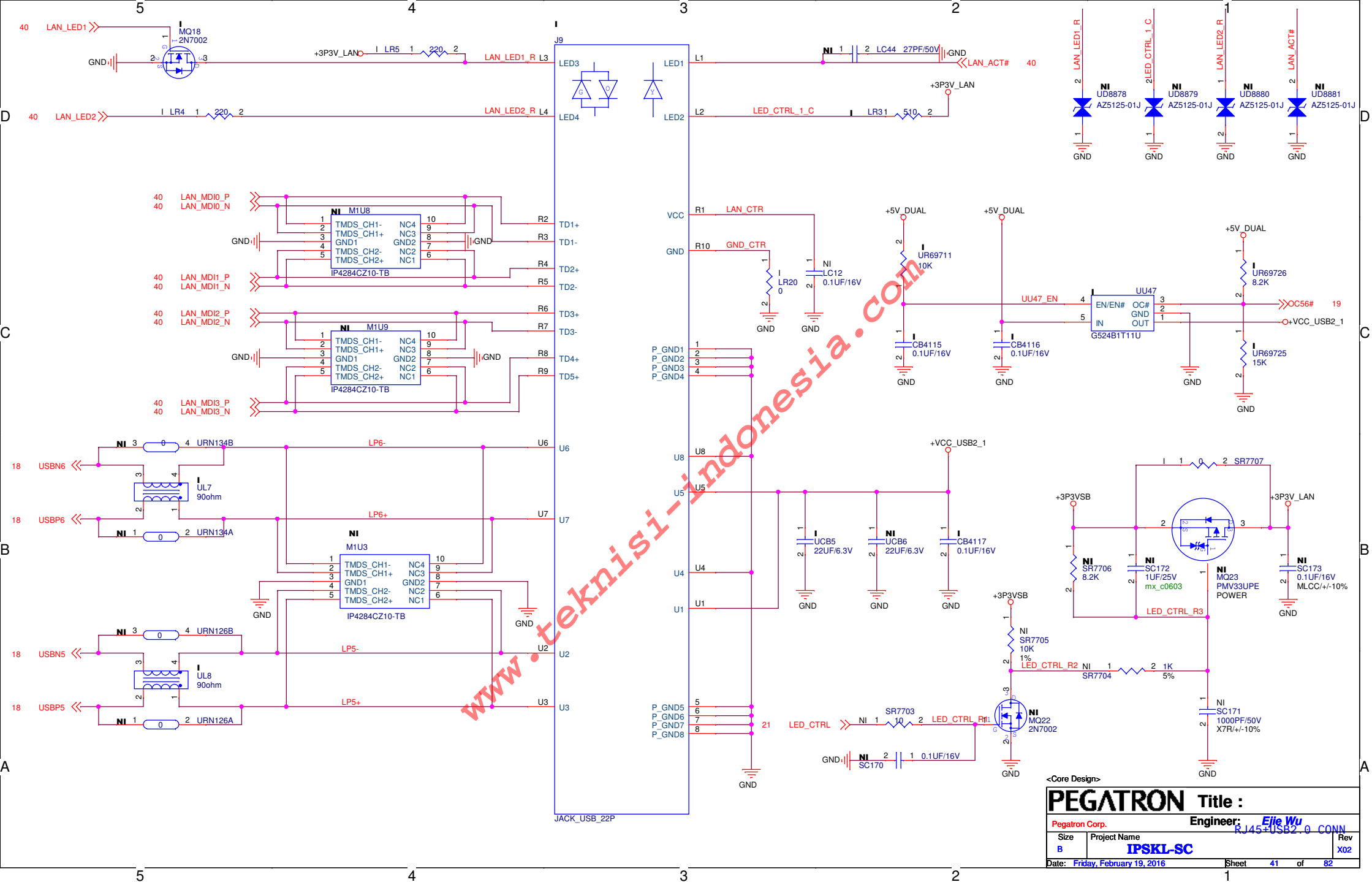
GND	TX1+	TX1-	VBUS	CC1	D+	D-	SBU1	VBUS	RX2-	RX2+	GND
GND	RX1+	RX1-	VBUS	SBU2	D-	D+	CC2	VBUS	TX2-	TX2+	GND

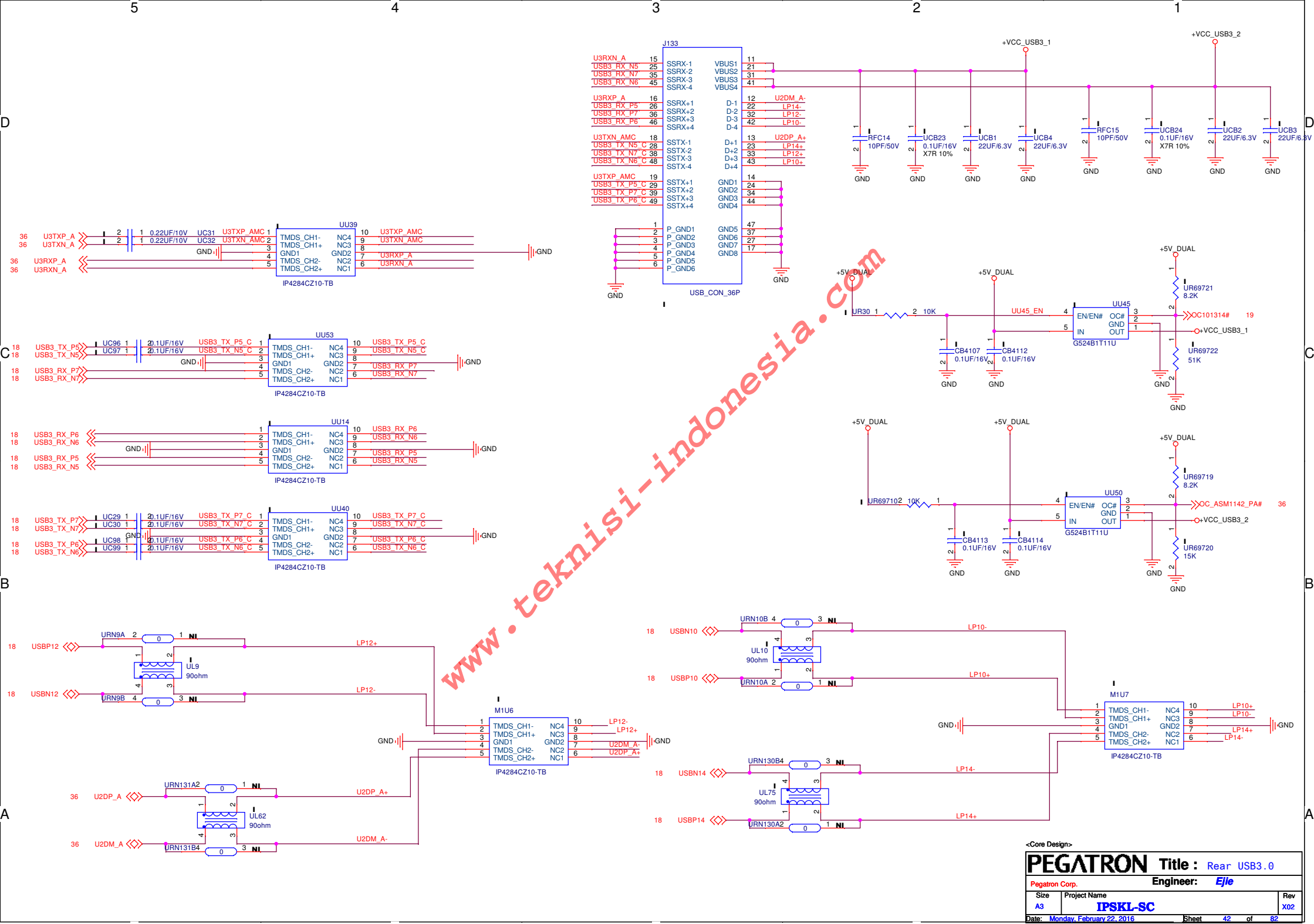


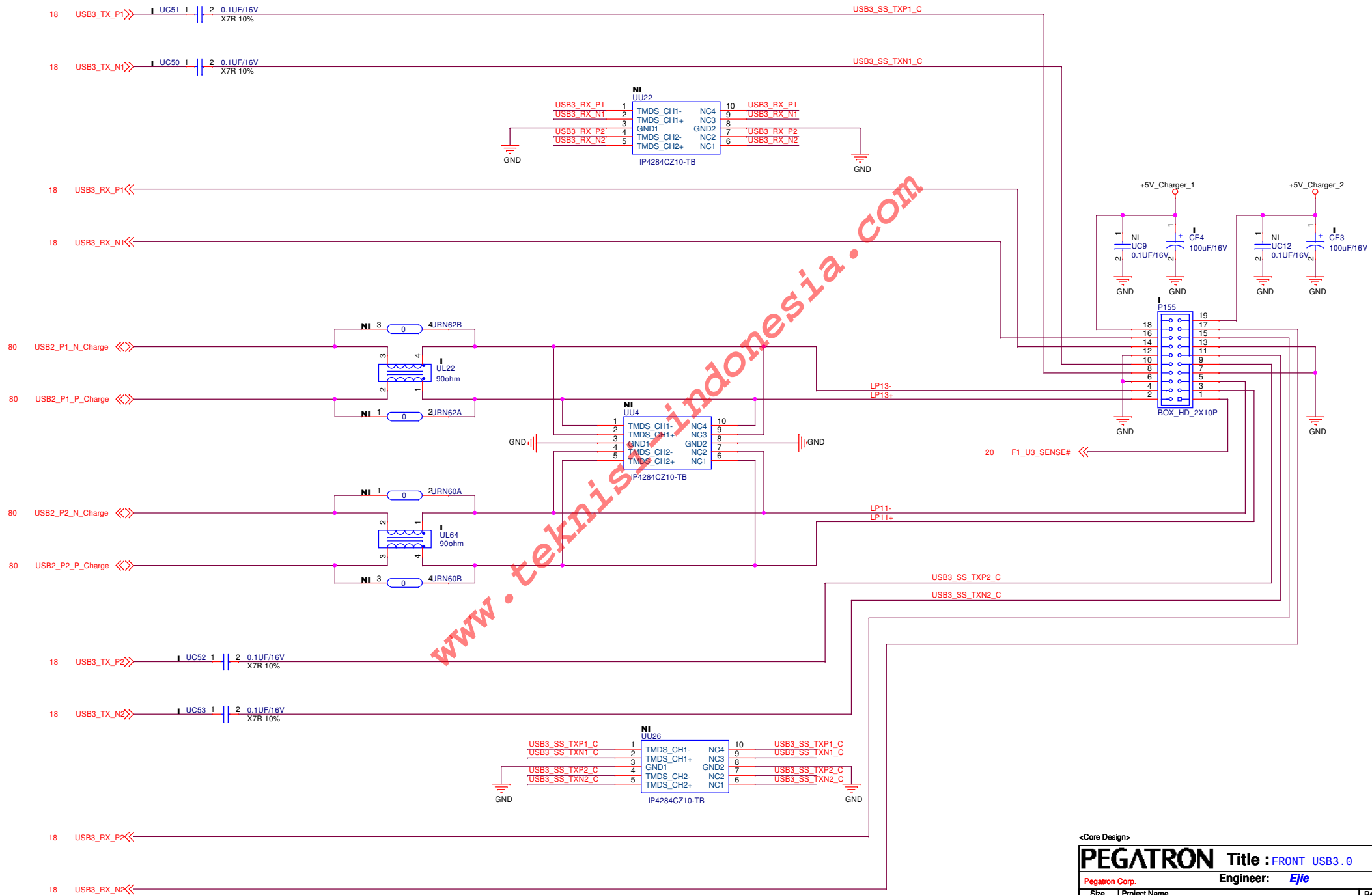


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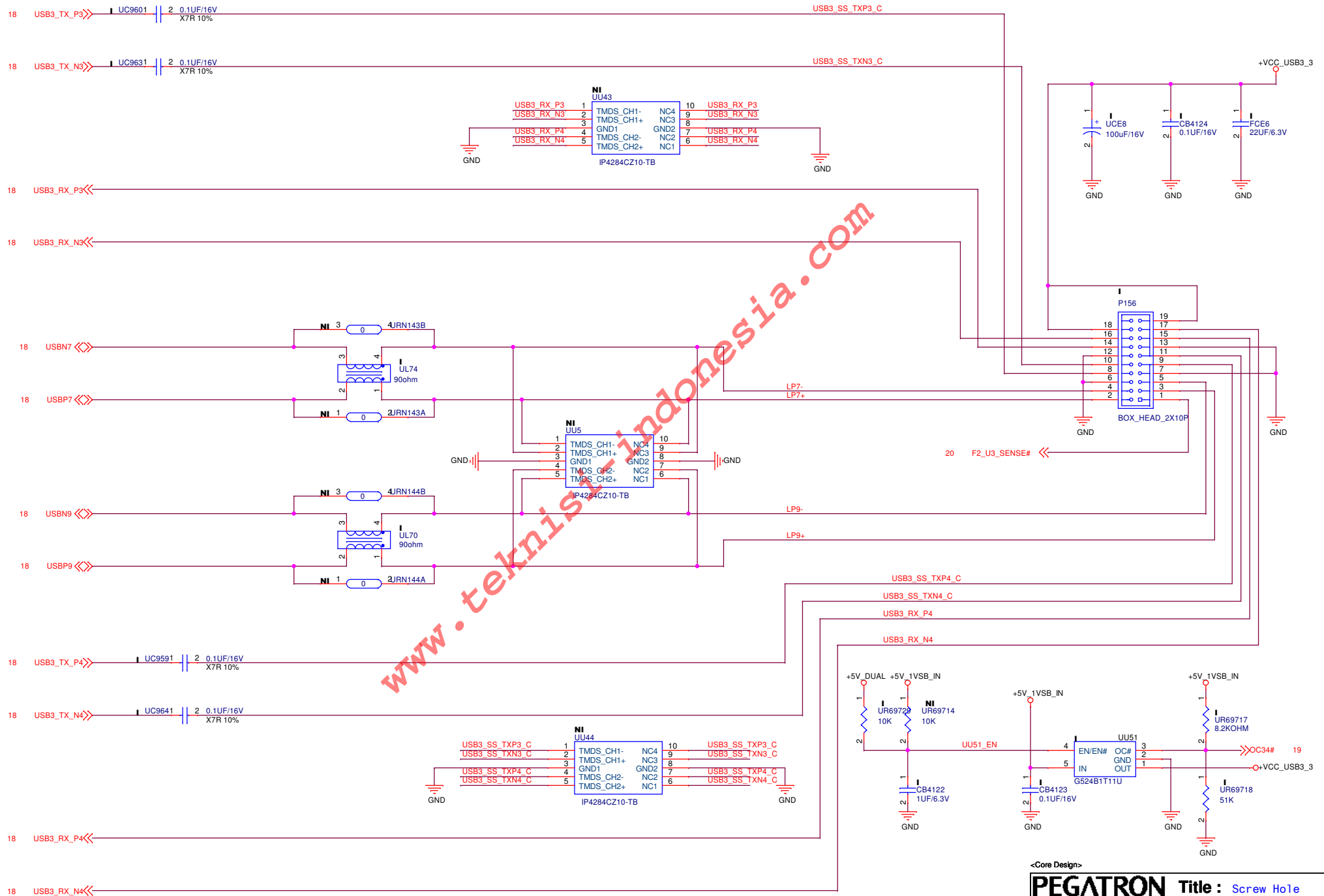
PEGATRON		Title : LAN_E2400	
Pegatron Corp.		Engineer: Ejie	
Size	Project Name	Rev	
A3	IPSKL-SC	X02	
Date: Wednesday, February 17, 2016		Sheet 40 of 82	







<Core Design>



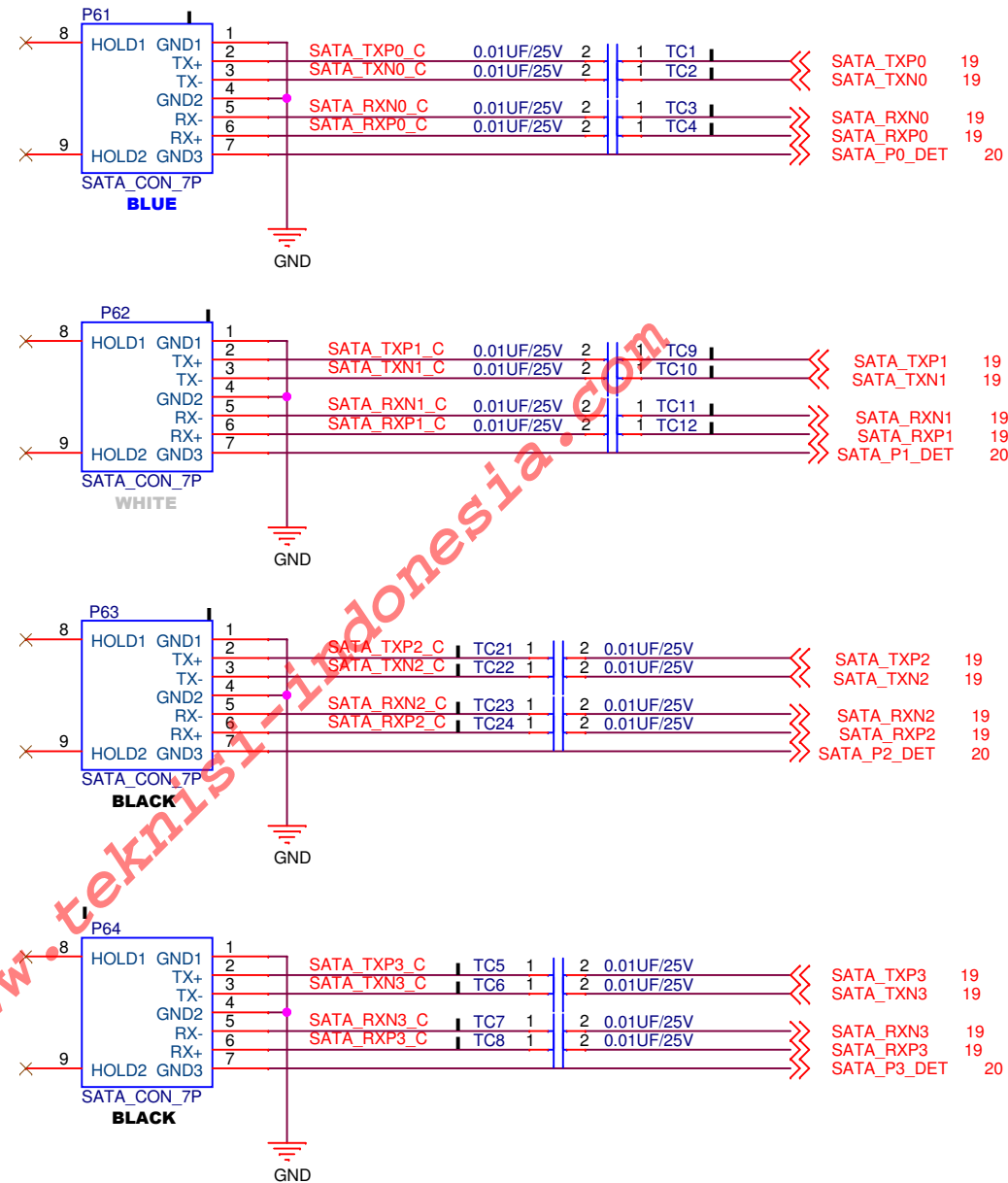
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PEGATRON Title : Screw Hole

Pegatron Corp. Engineer: Eje

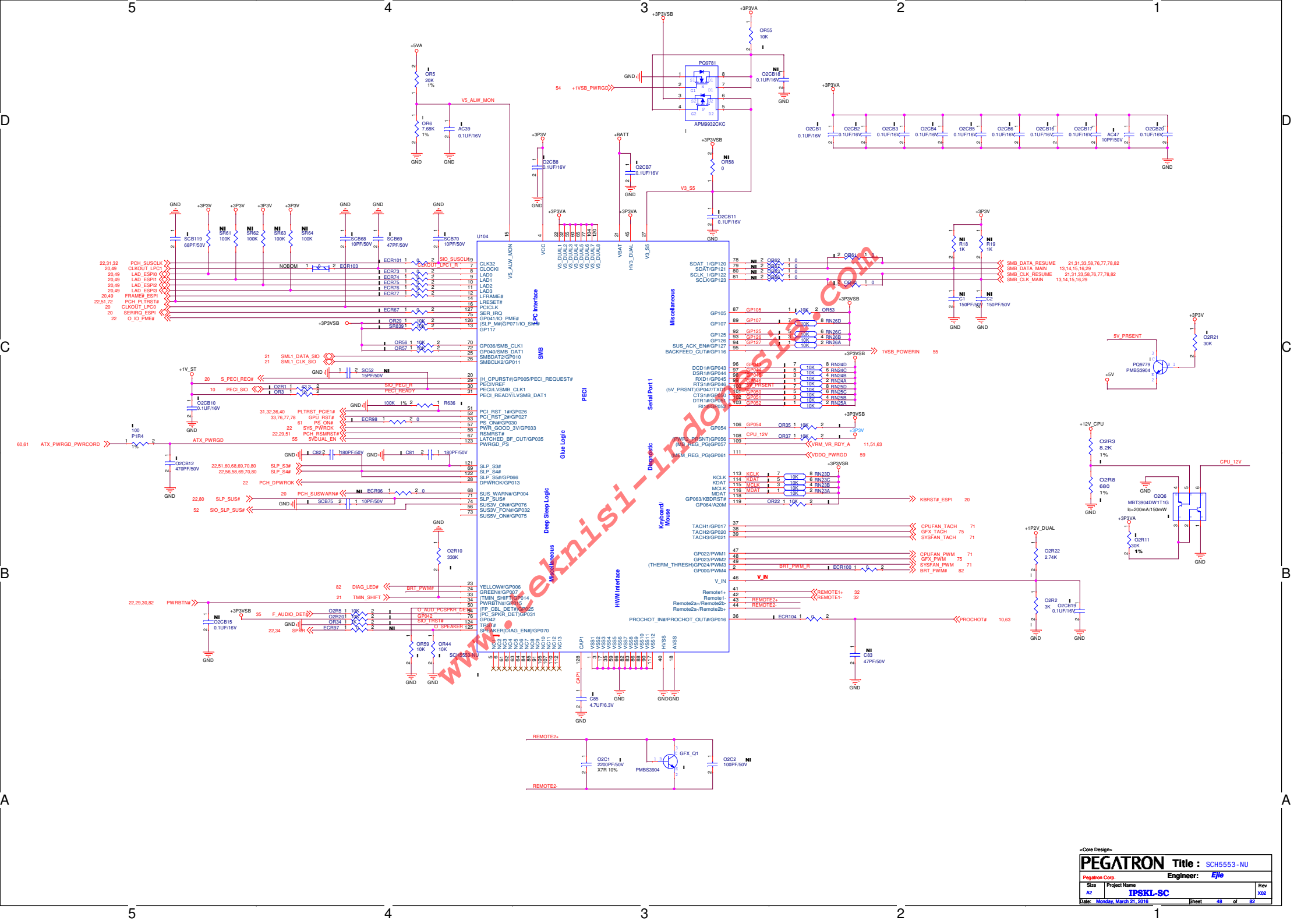
Size A3	Project Name IPSKL-SC	Rev X02
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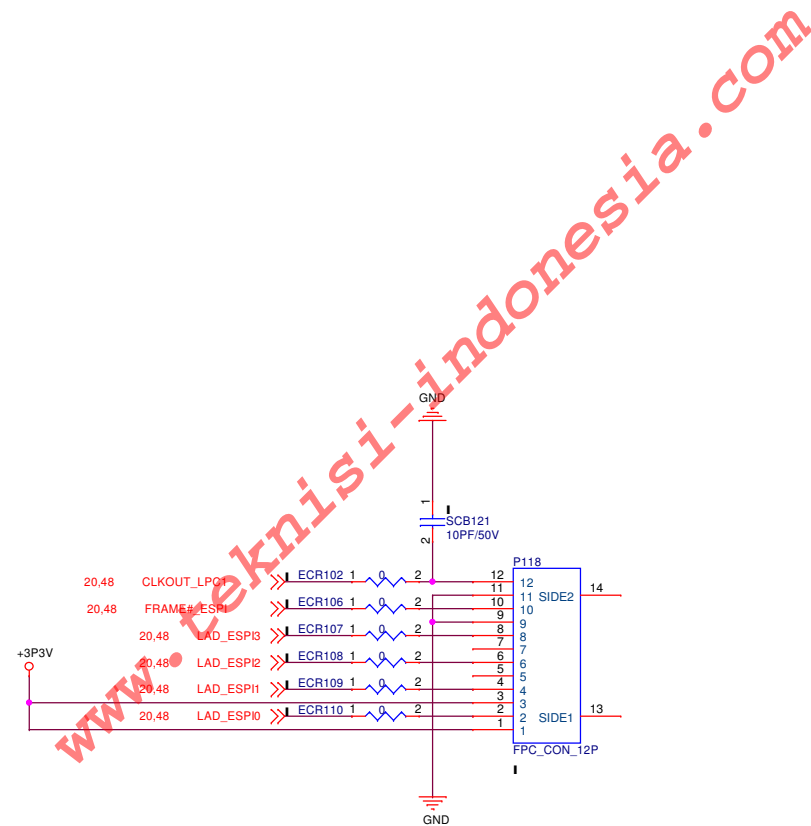
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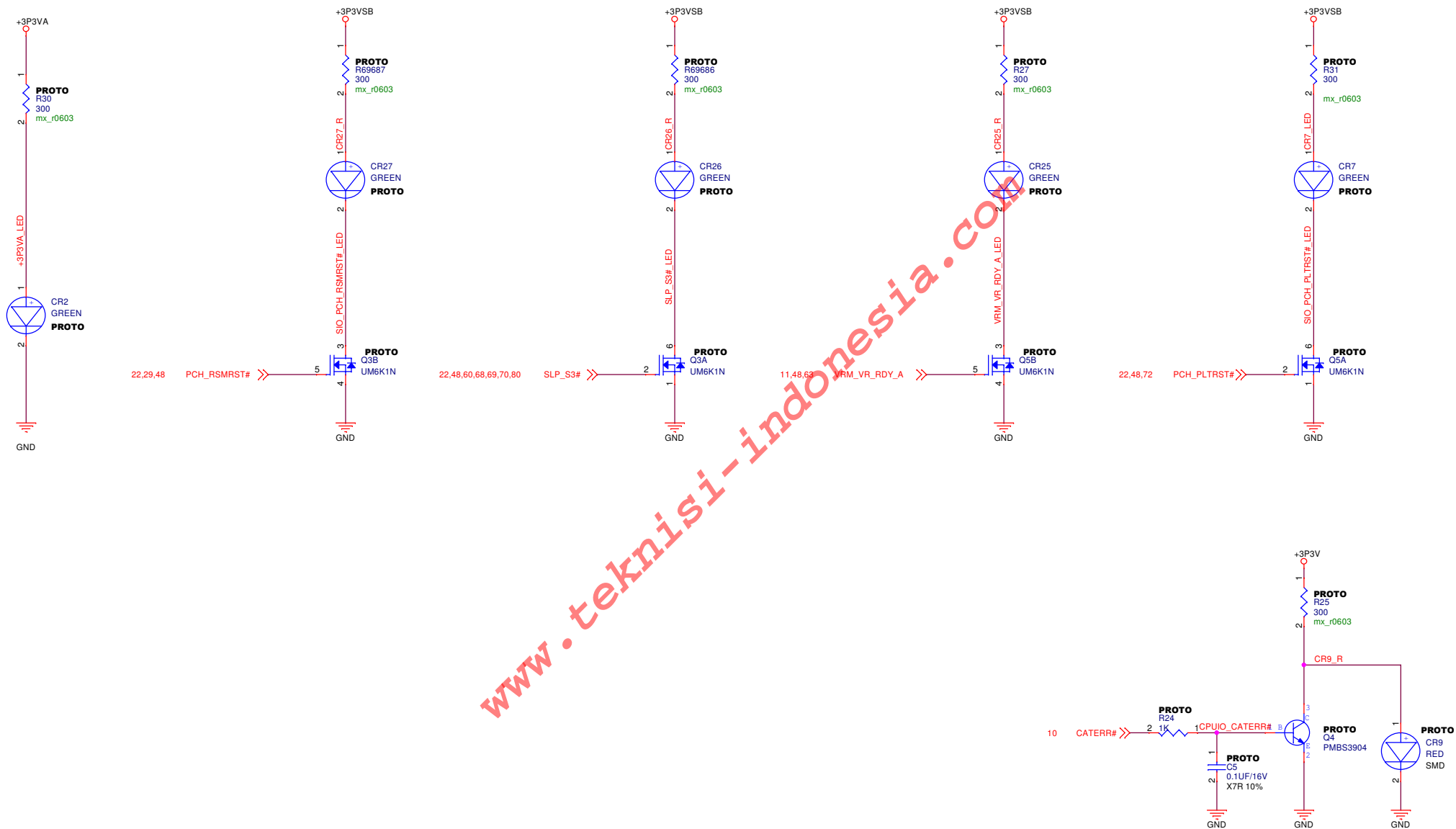
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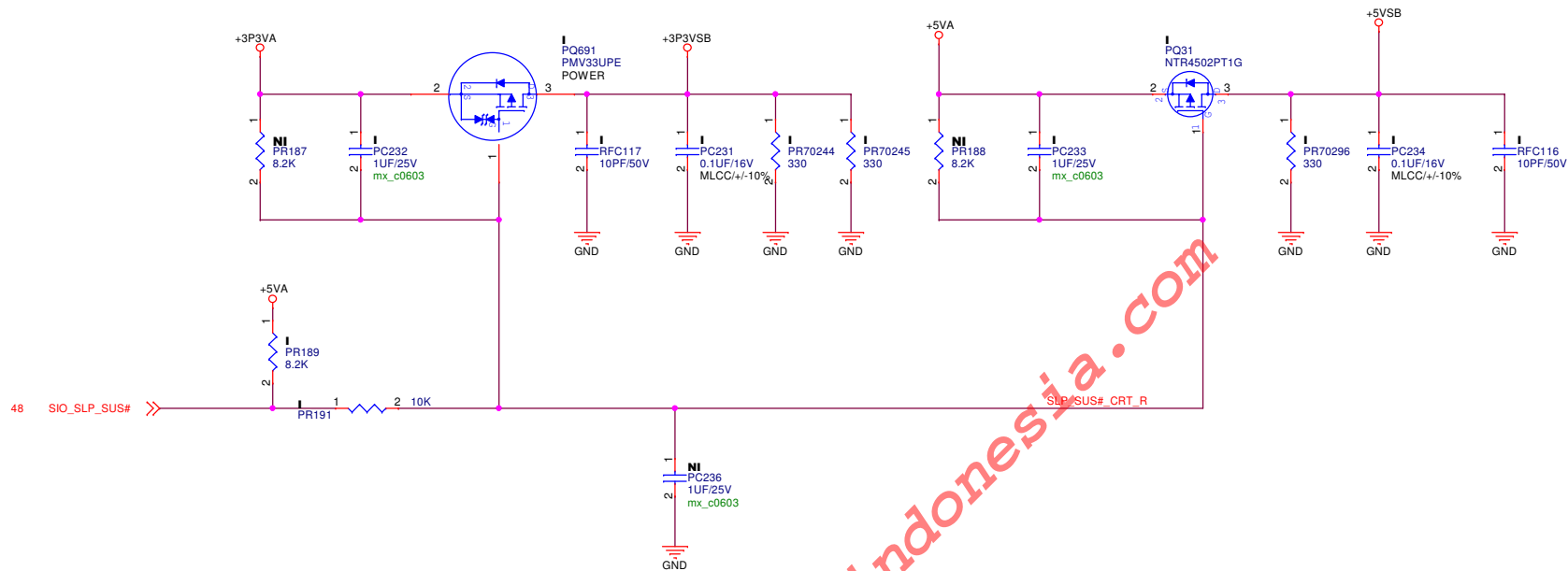
PEGATRON		Title : SATA CONN	
Pegatron Corp.		Engineer: Ejie	
Size A4	Project Name IPSKL-SC		Rev X02
Date: Wednesday, February 17, 2016		Sheet	45 of 82





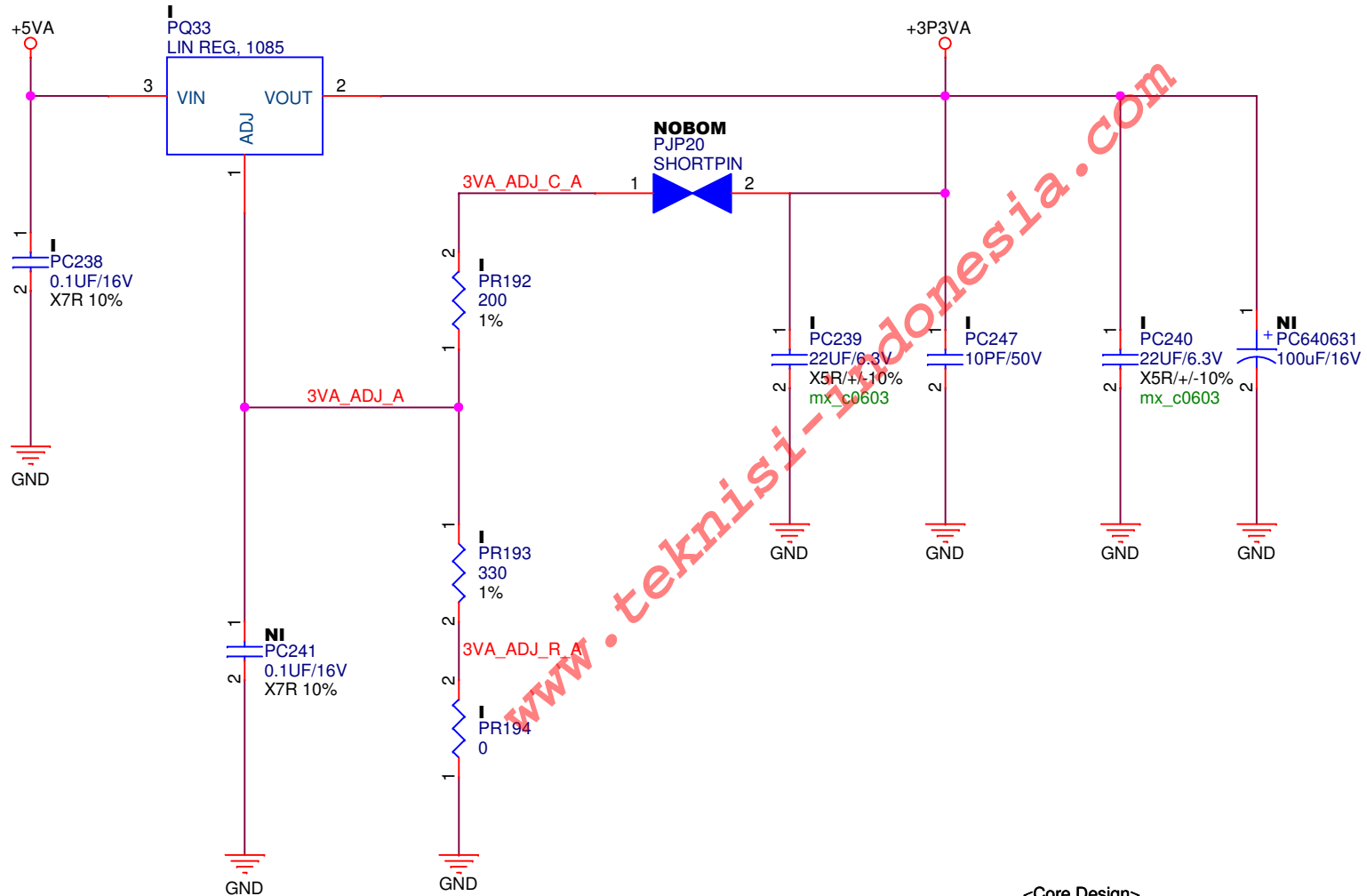
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<Core Design>

PEGATRON		Title : +3V / 5VSB / +3VA	
Pegatron Corp.		Engineer: Ejie	
Size A03	Project Name IPSKL-SC		Rev X02
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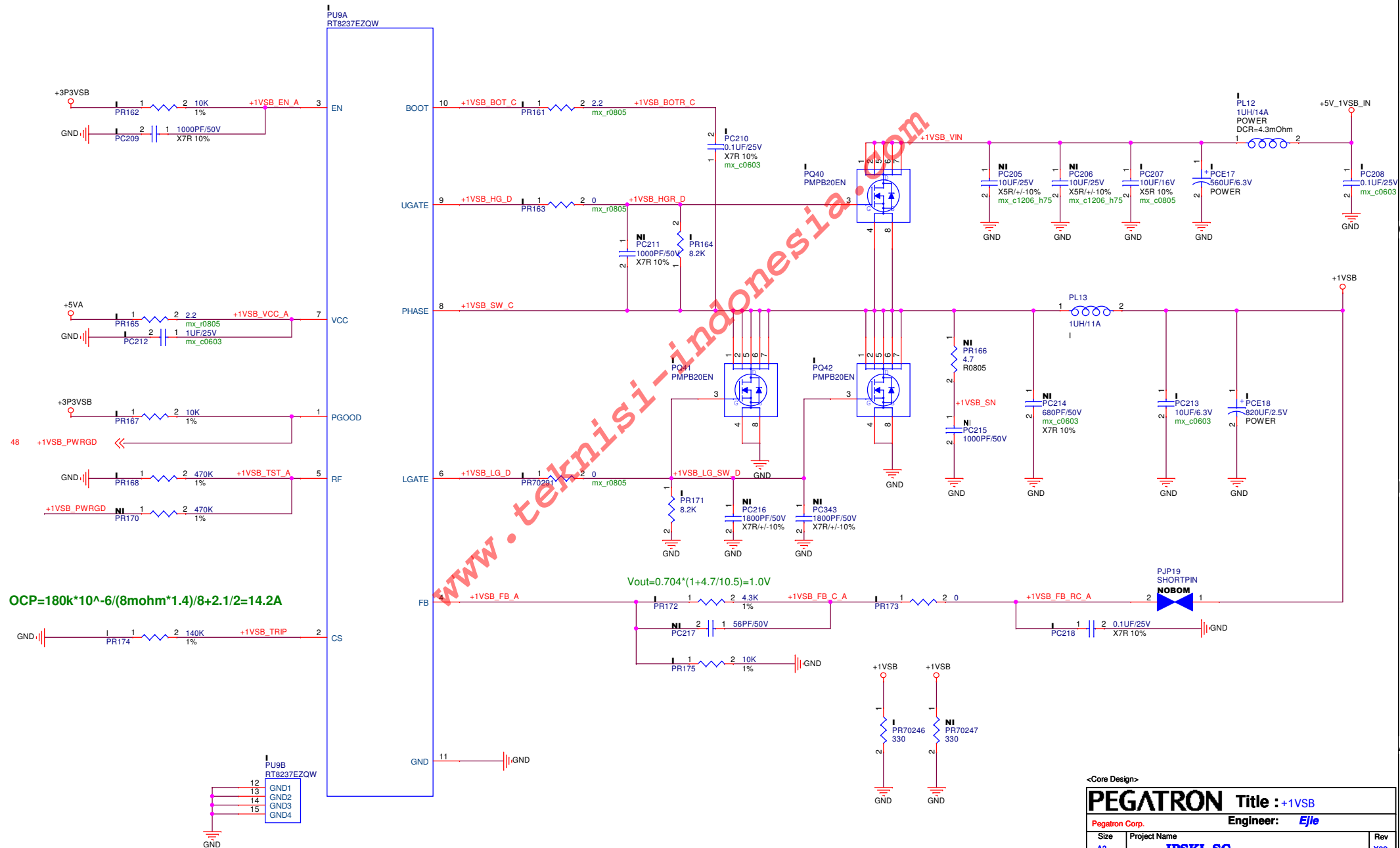


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Title		
<Title>		
Size	Document Number	Rev
A	<Doc>	<Rev Code>
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R_{RF} (k Ω)	Switching Frequency (kHz)
470k Ω	290
200k Ω	340
100k Ω	380
39k Ω	430

Note : For DEM, connect R_{RF} to GND; for CCM, connect R_{RF} to PGOOD.



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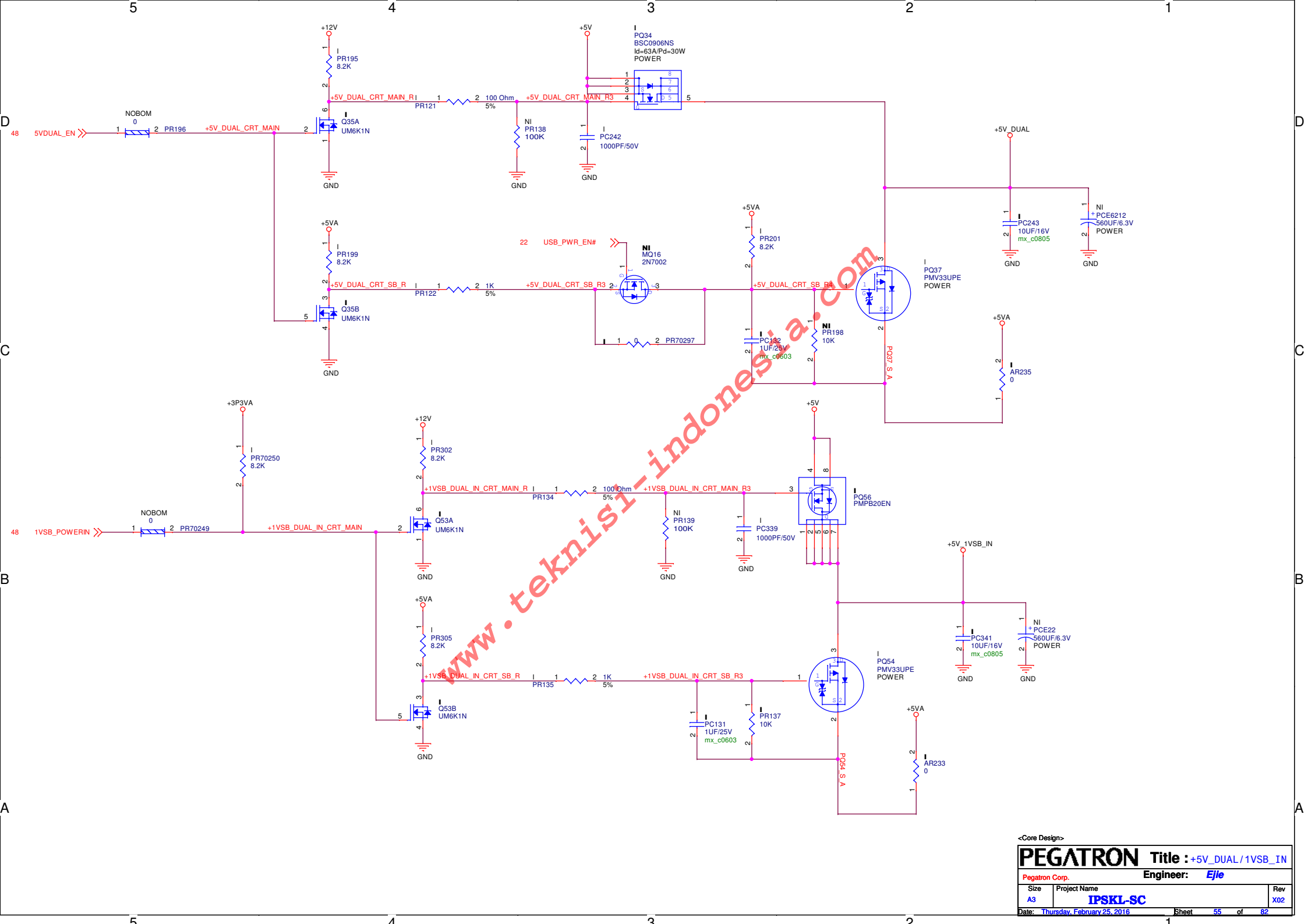
PEGATRON Title : +1VSB

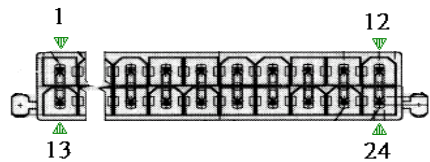
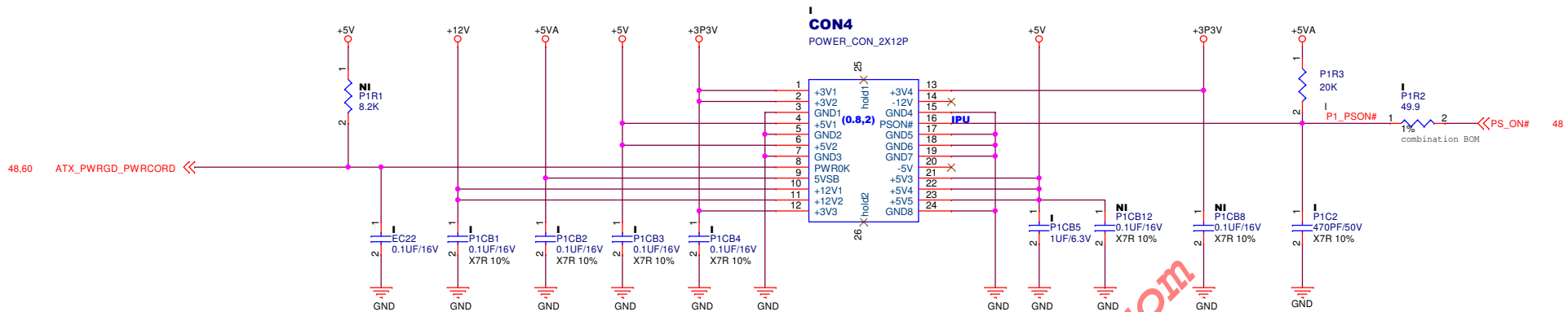
Pegatron Corp. **Engineer:** *Ejle*

Size	Project Name
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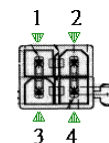
A3	IPSKL-SC
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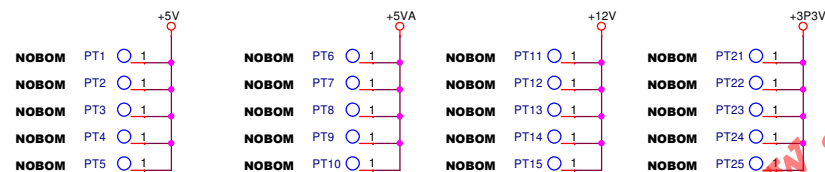




TOP SIDE VIEW

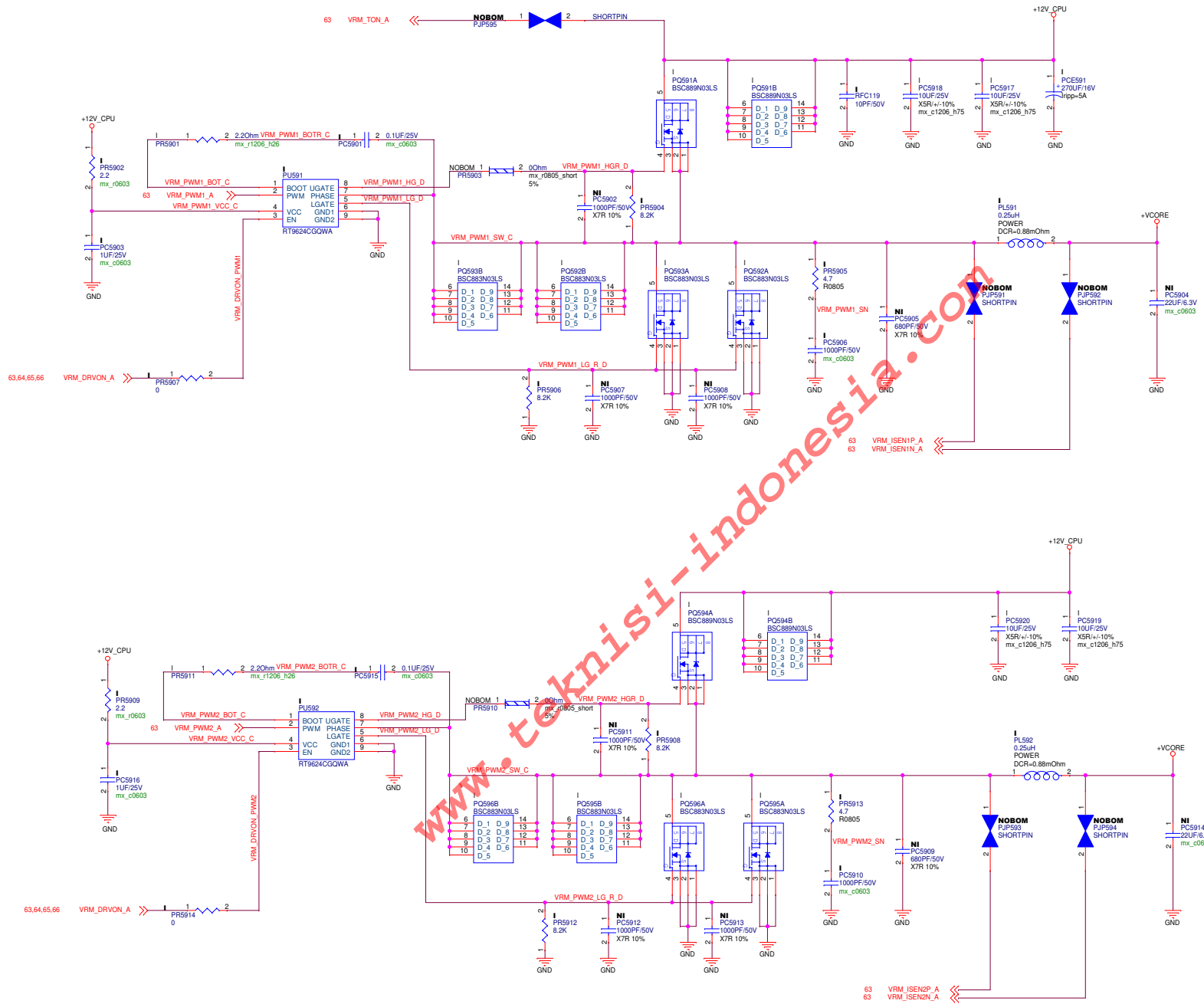


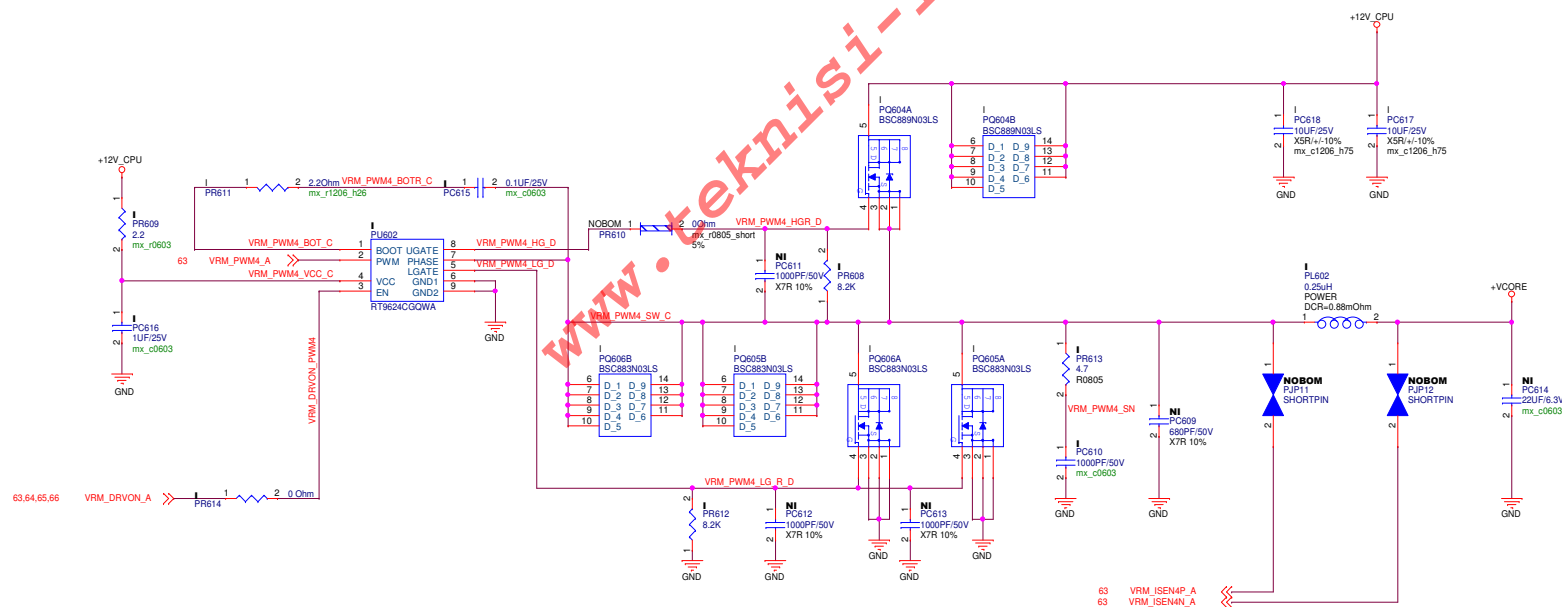
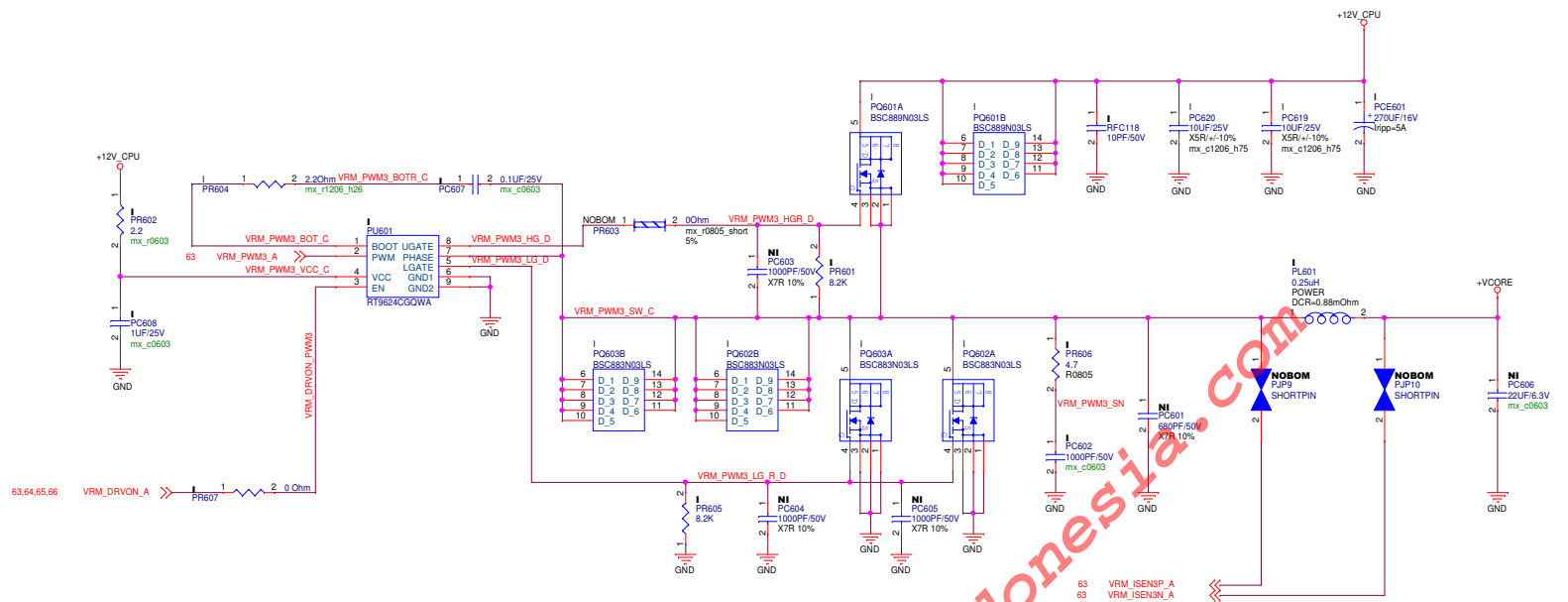
TOP SIDE VIEW

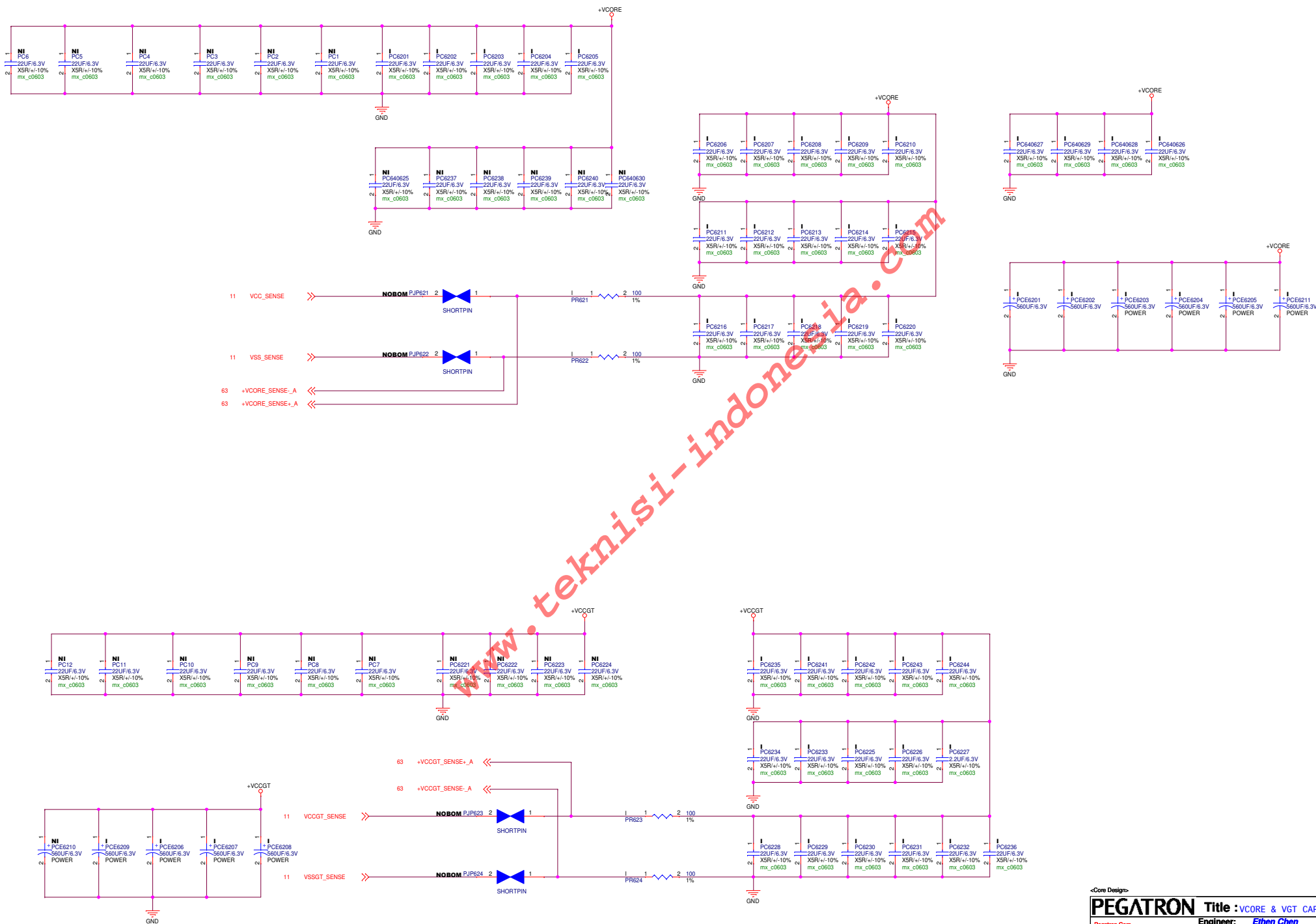


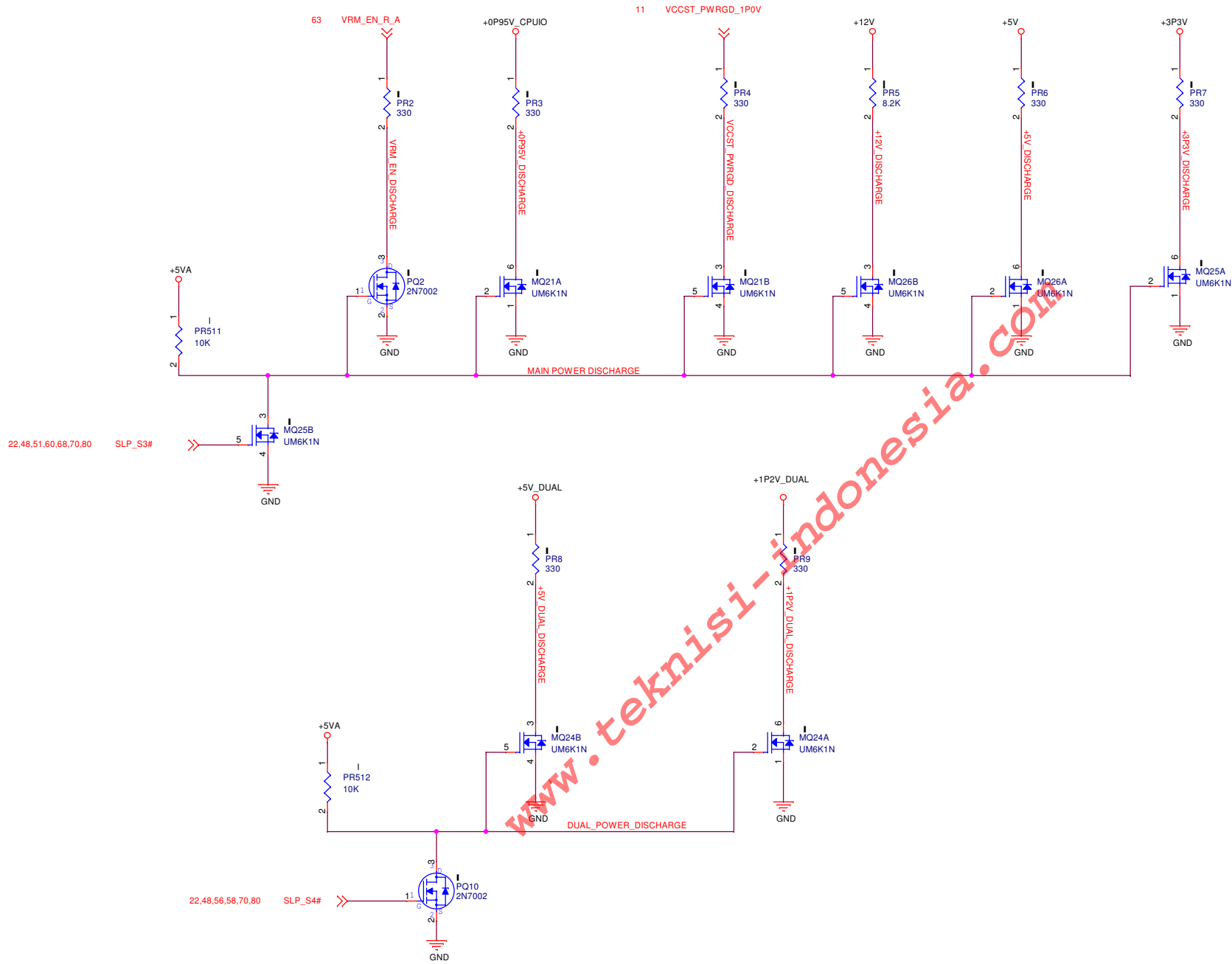
Node	Goal Q'ty
+5V	5
+5VA	5
+12V	5
-12V	5
+3V	5
+Vcore	10
+GND	15
+12V_CPU	10

<Core Design>





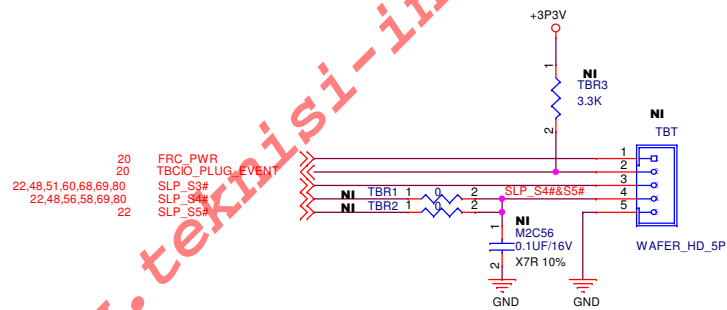




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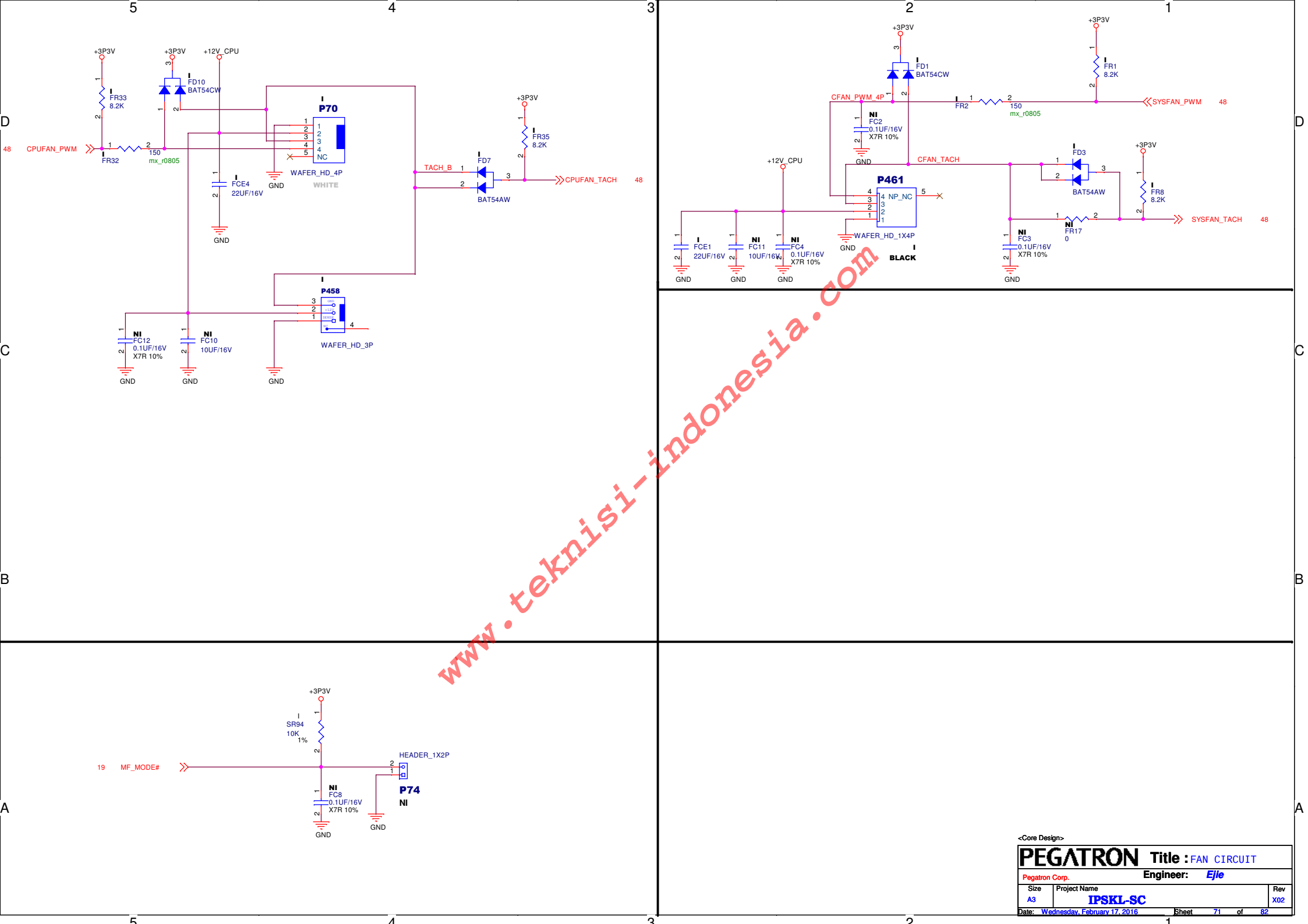
PEGATRON		Title : xxxx	
Pegatron Corp.		Engineer: Ejle	
Size A3	Project Name IPSKL-SC		Rev X02
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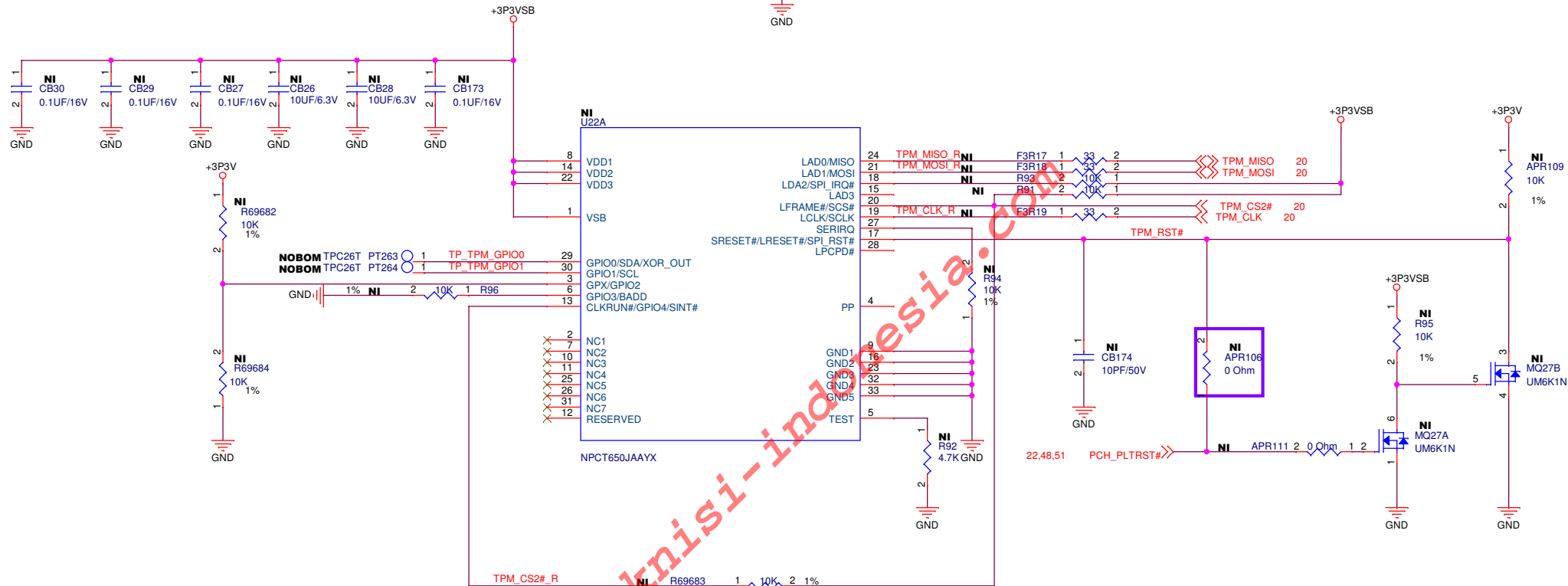
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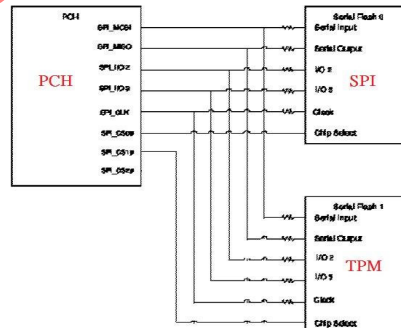
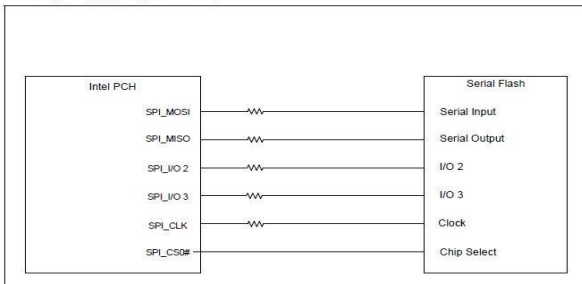
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PEGATRON		Title : NUT	
Pegatron Corp.		Engineer: Ejle	
Size	Project Name		Rev
A3	IPSKL-SC		X02
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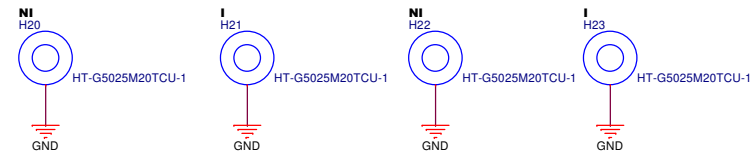
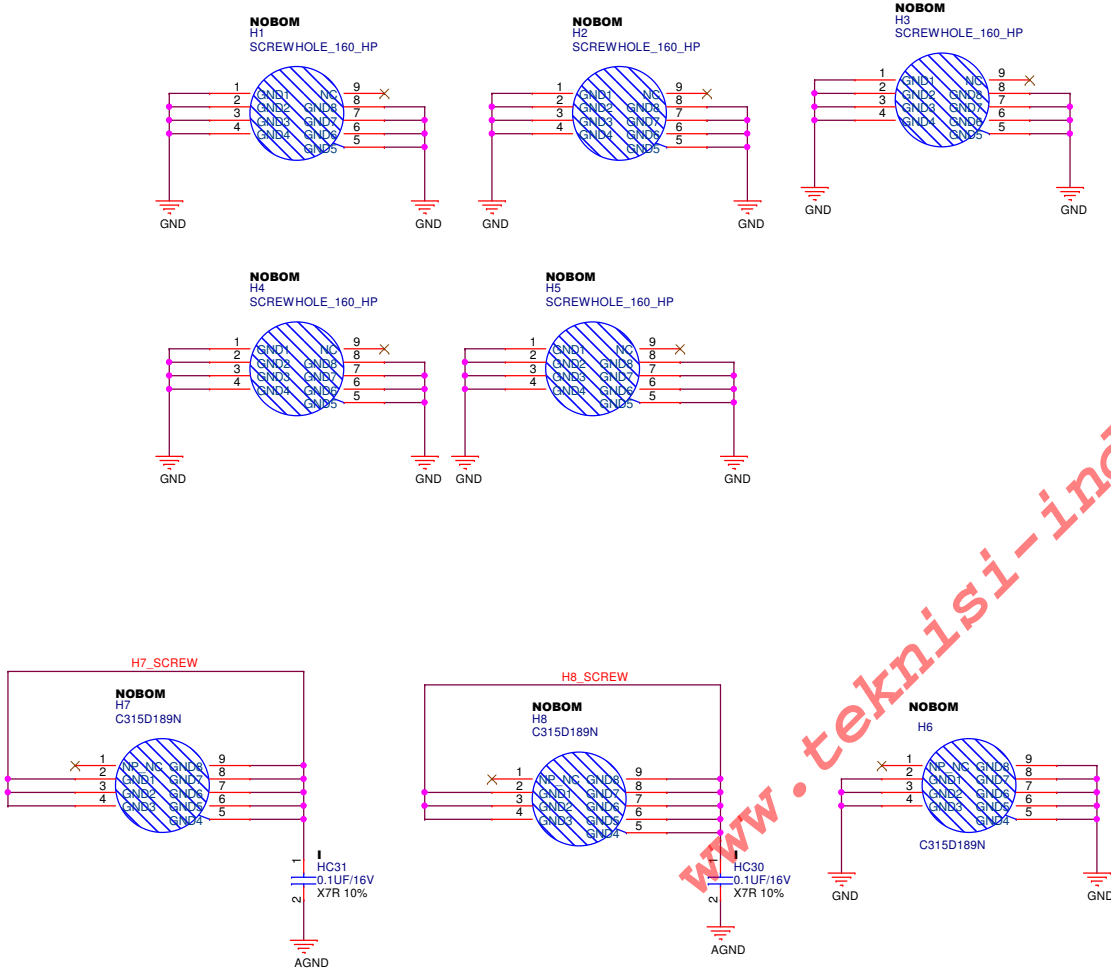


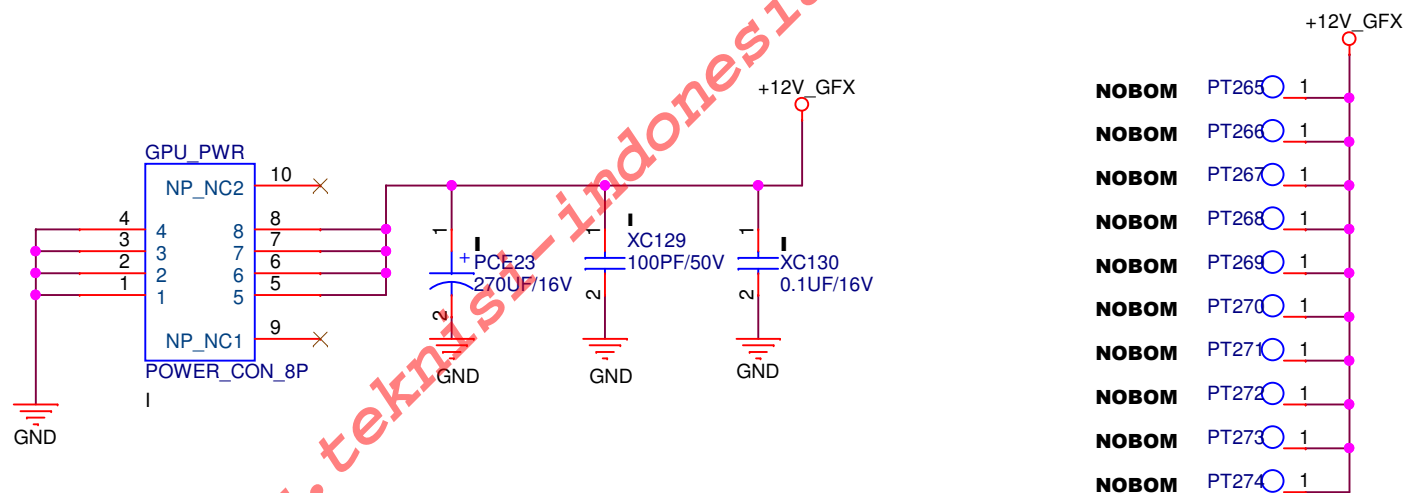
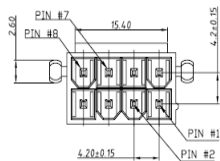


SPI Topology (Single Device)



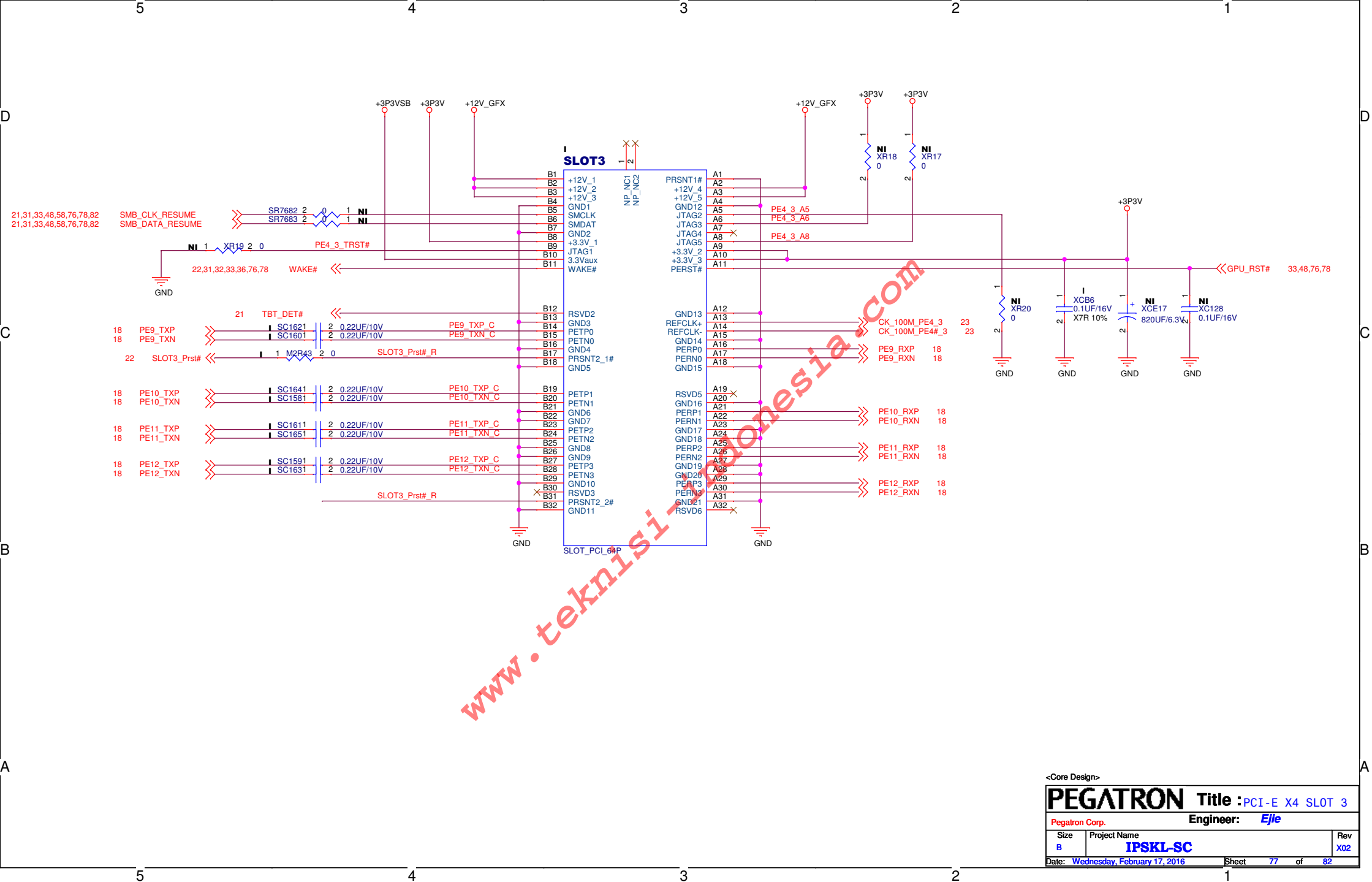
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PEGATRON		Title : TPM	
Pegatron Corp.		Engineer: Ejl	
Size B	Project Name IPSKL-SC		Rev X02
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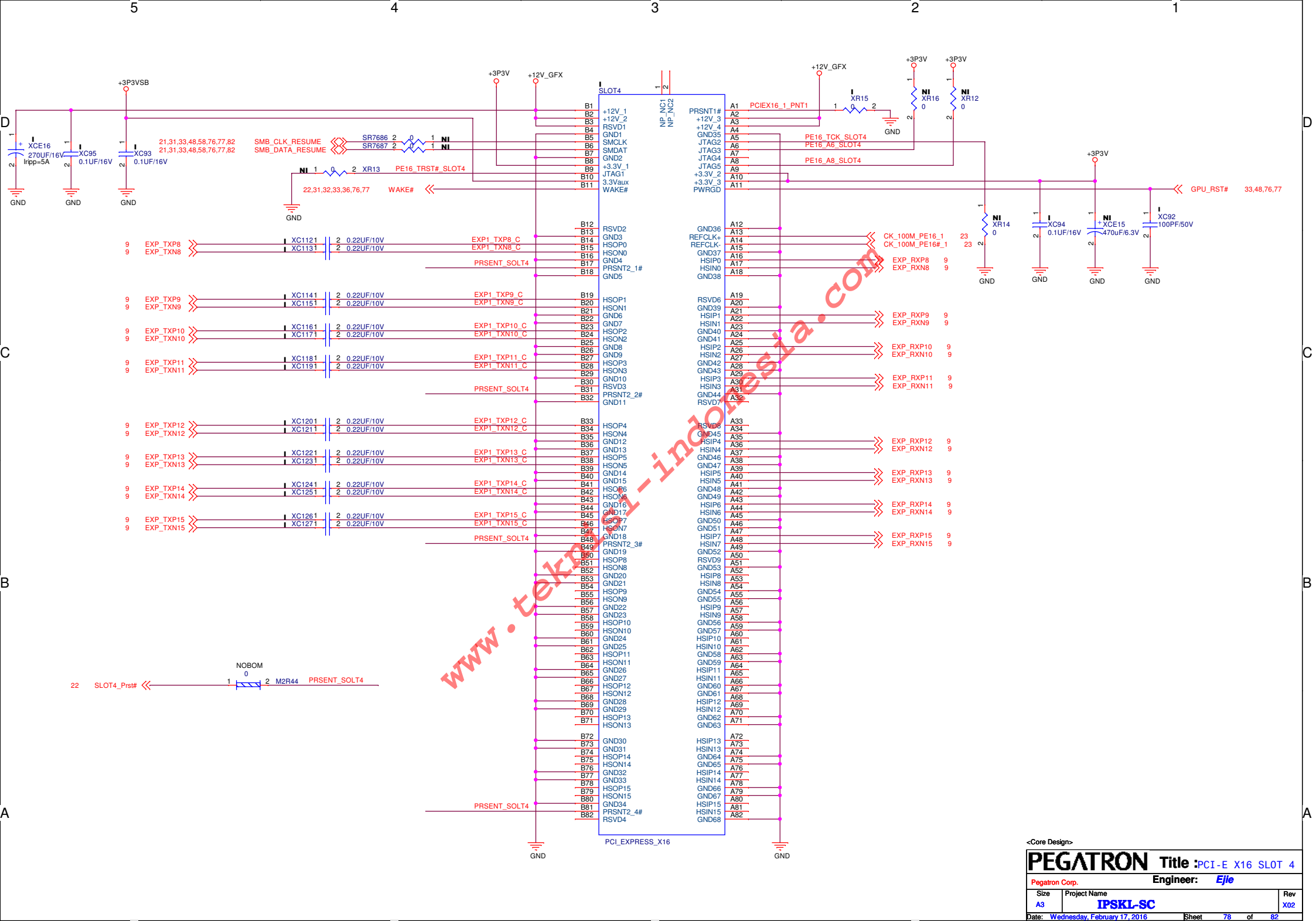


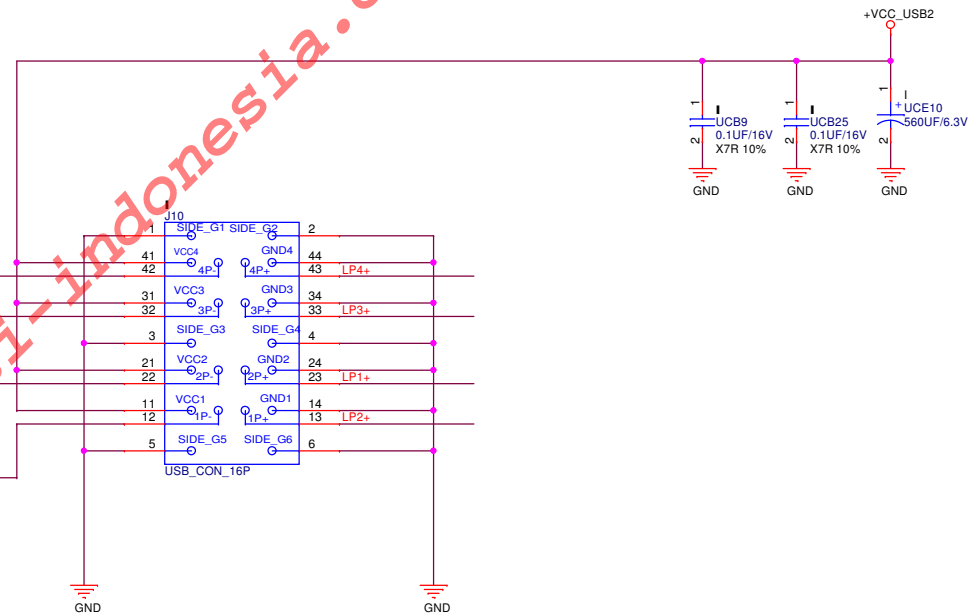
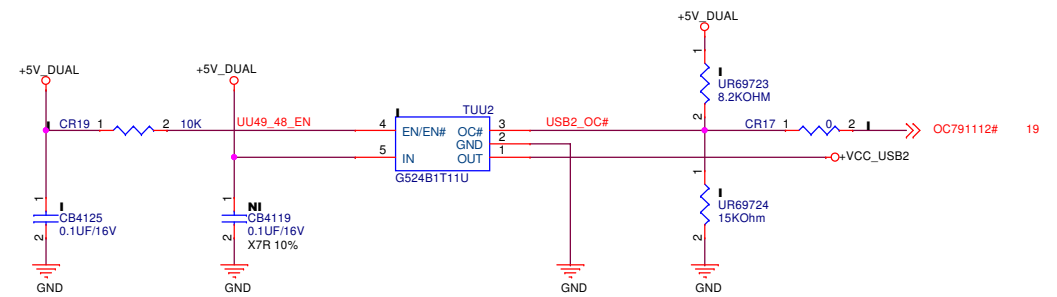
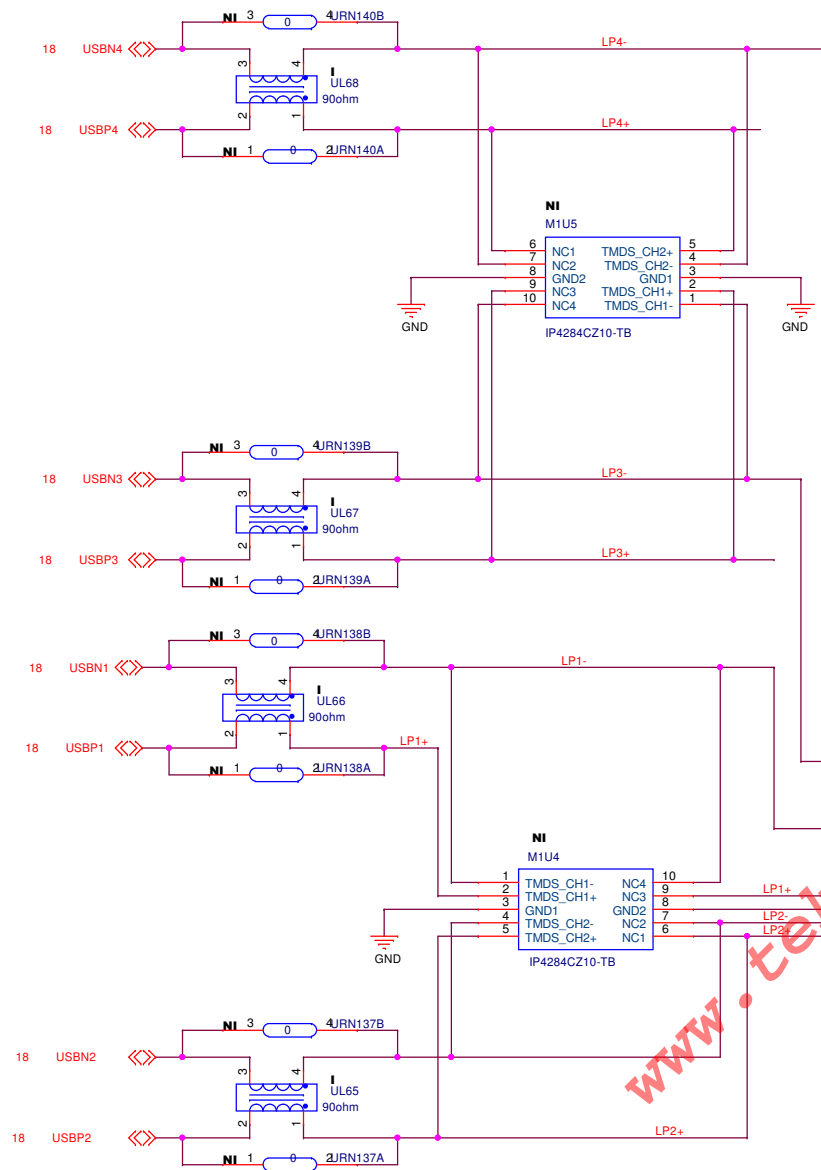


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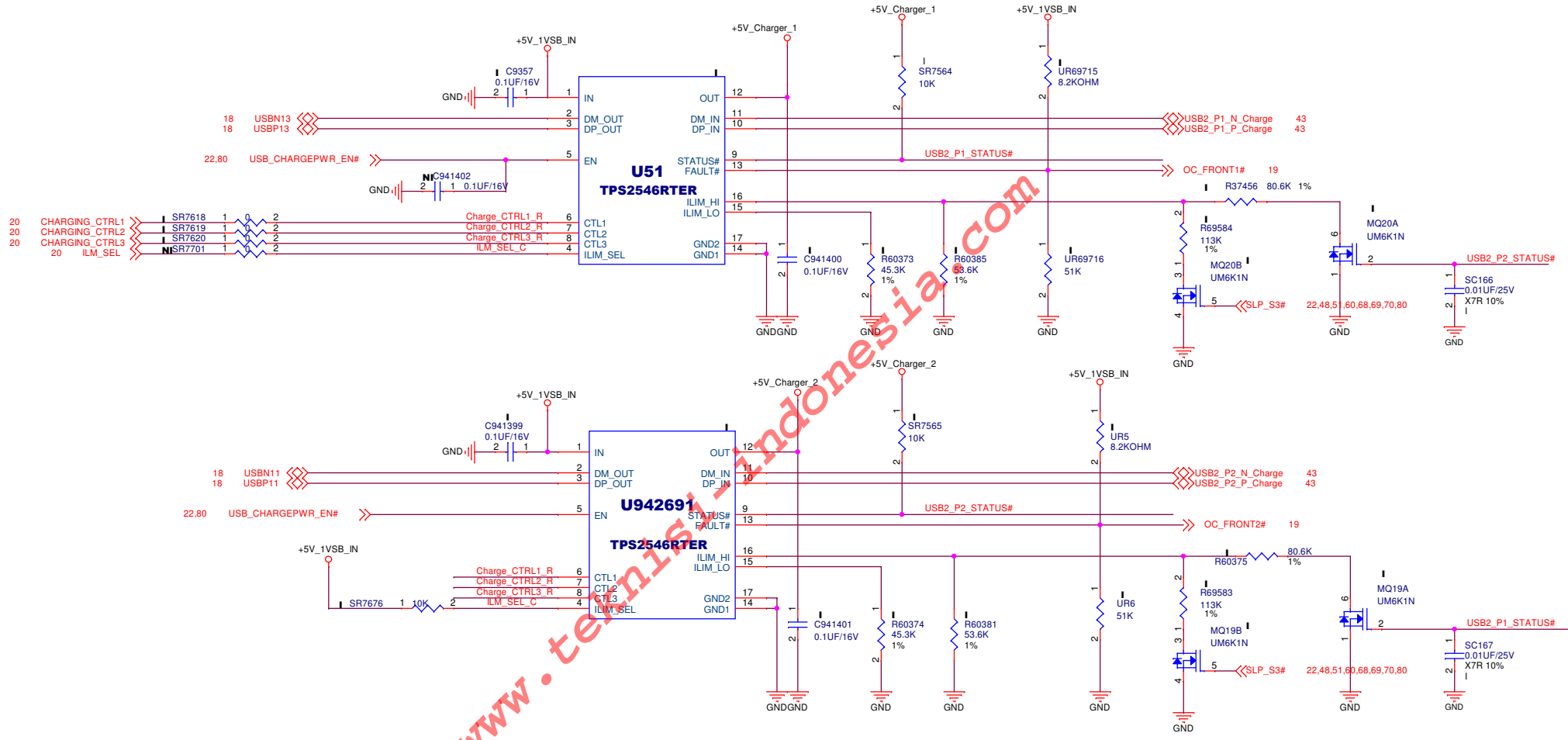
PEGATRON		Title : GPU_PWR	
Pegatron Corp.		Engineer: Ejie	
Size A	Project Name IPSKL-SC		Rev X02
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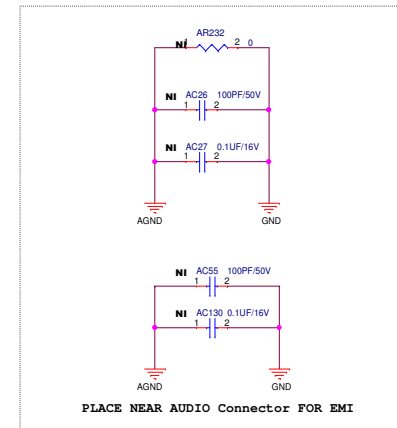
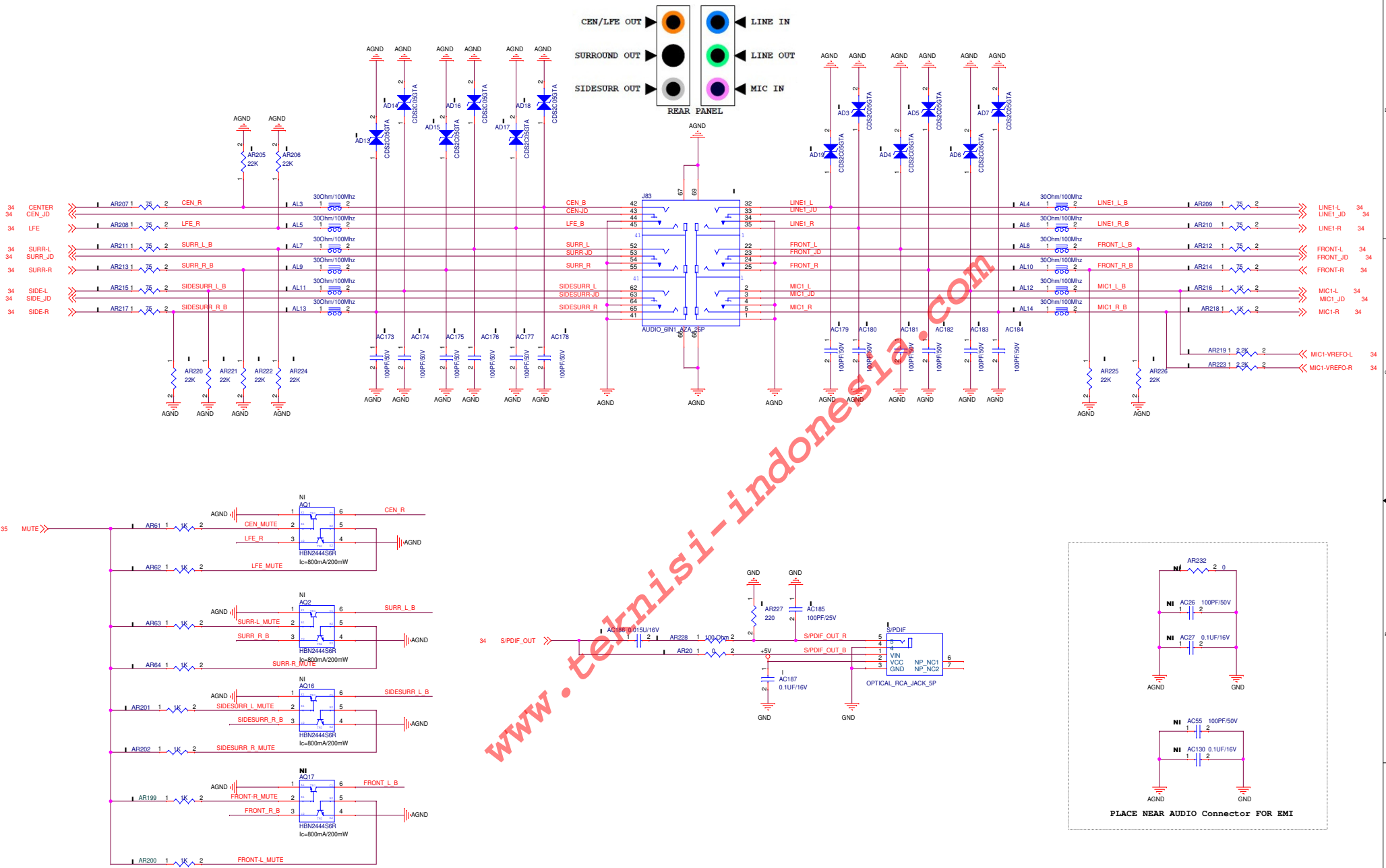


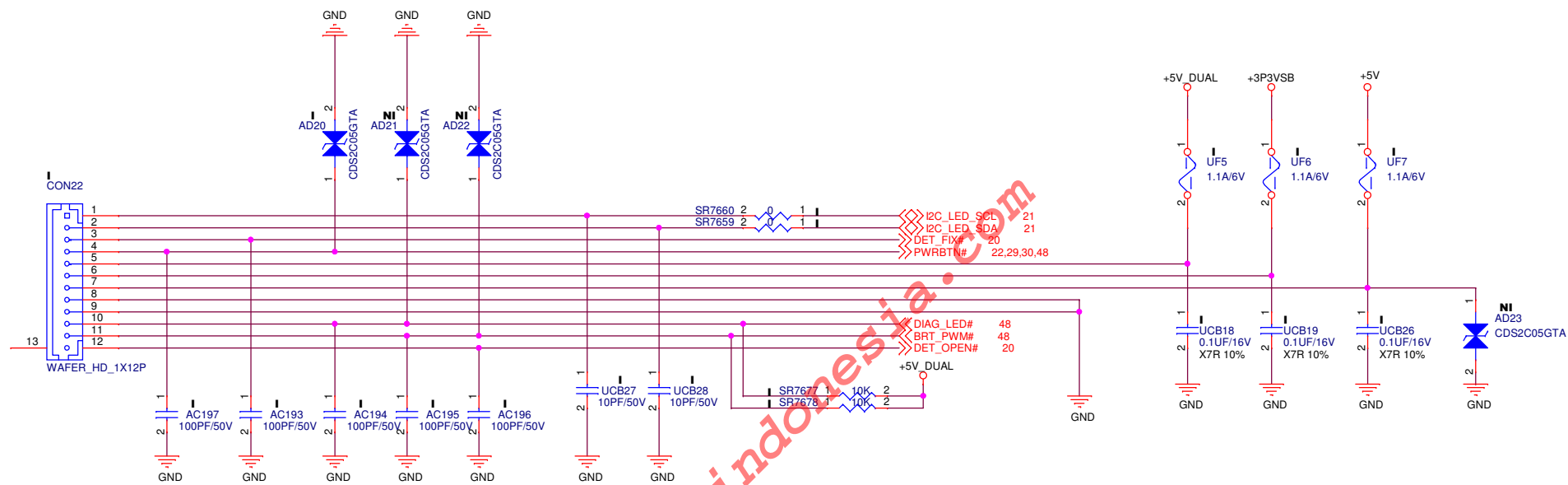


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S0=53.6k//113k//80.6=2A (single port charge)
S0=53.6k//113k=1.4A (dual port charge)
S345=53.6k//80.6k=1.5A (single port charge)
S345=53.6k=0.9A (dual port charge)
45.3K=1.1A (status# threshold)





<Core Design>			
PEGATRON		Title : LED DRIVER	
Pegatron Corp.		Engineer: Ejle	
Size B	Project Name IPSKL-SC		Rev X02
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